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July 2014

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Device Embedding in PCBs: Evolution or Revolution?

by Michael Weinhold, page 16

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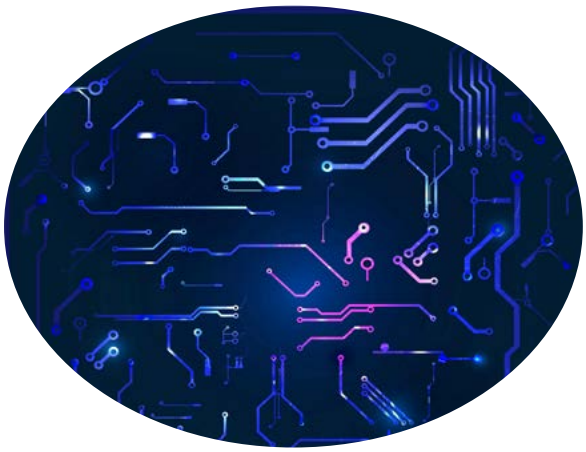

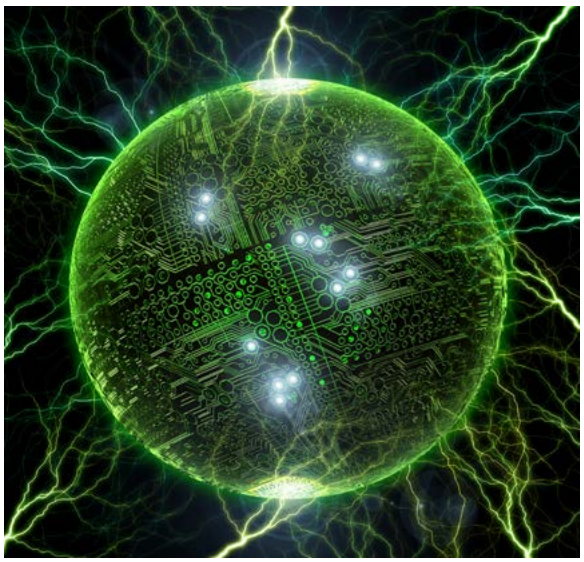

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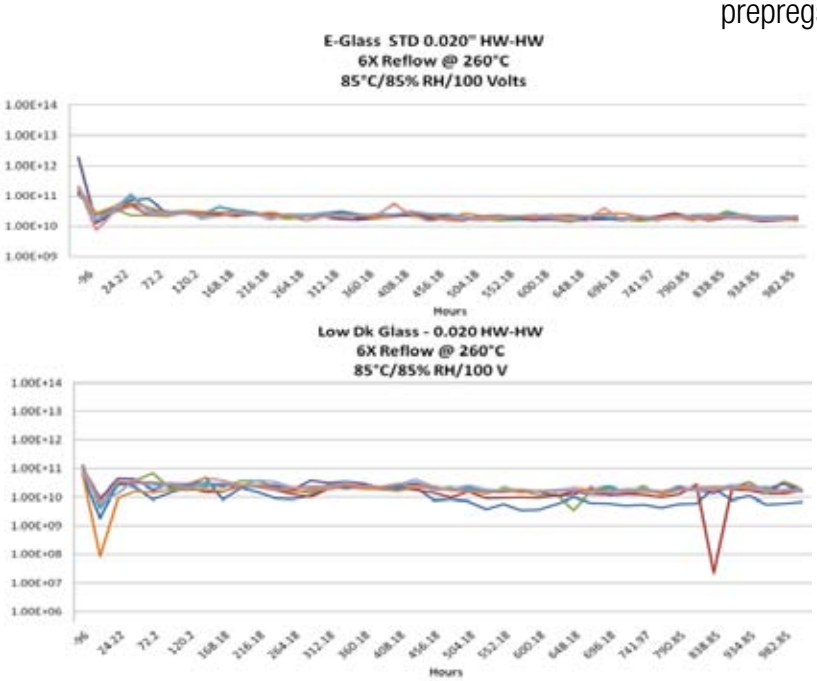

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Electronic Assembly with Solder: an Unblinking Look at "The Devil We Know"

by Joe Fjelstad
VERDANT ELECTRONICS

Solder is unquestionably highly practical technology for joining metals, and carries with it a long history. Its roots go back more than 2,000 years. Somewhere in the distant past, one of our more clever and observant ancestors chanced to create an alloy of tin and lead that melted at a low temperature. They or someone who learned of their discovery found that this unique combination of elements could be used to join pieces of metal together. This combination of chance observation and applied imagination has proven a key development in the technological history of mankind. Those in the electronics industry of today are very familiar with this ancient technology and today it is still the method of choice for making electronic assemblies of every sort. The only fly in the ointment is that the EU parliament, in a mad rush to try to look "green," took the emotional and scientifically ill-advised position that lead needed to be banned from electronic solders.

Sadly, there was never presented a credible piece of scientific evidence that any user had ever been harmed by tin-lead solder in electronic equipment. Nor could they prove their assertion that it would be a risk to ground water. That said, it is true that greed and complete mismanagement of electronic waste boarding on criminal behavior, has resulted in physical illness and environmental harm in areas of the world where uncontrolled recycling was being carried out by uneducated individuals. While all

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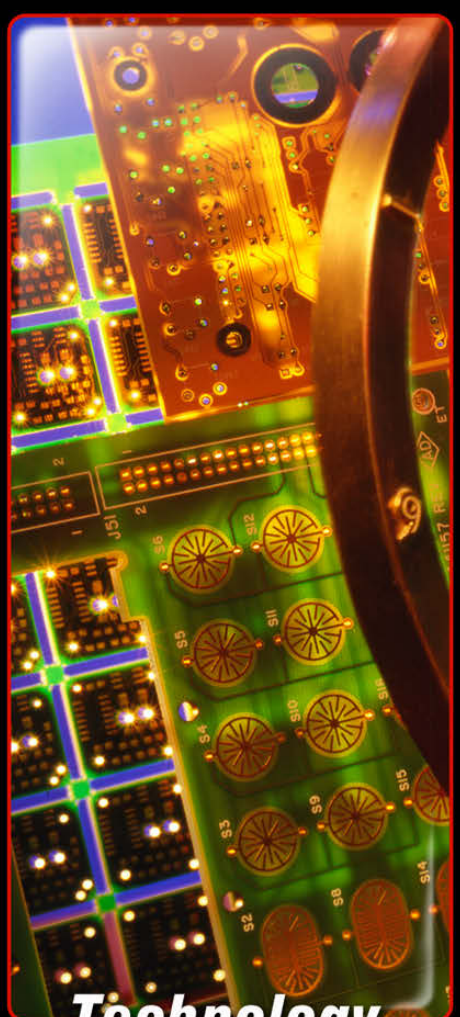

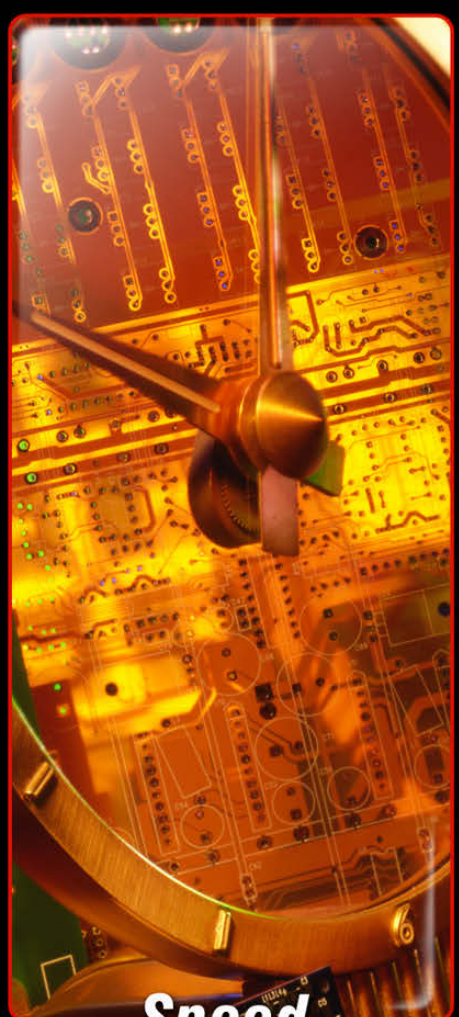

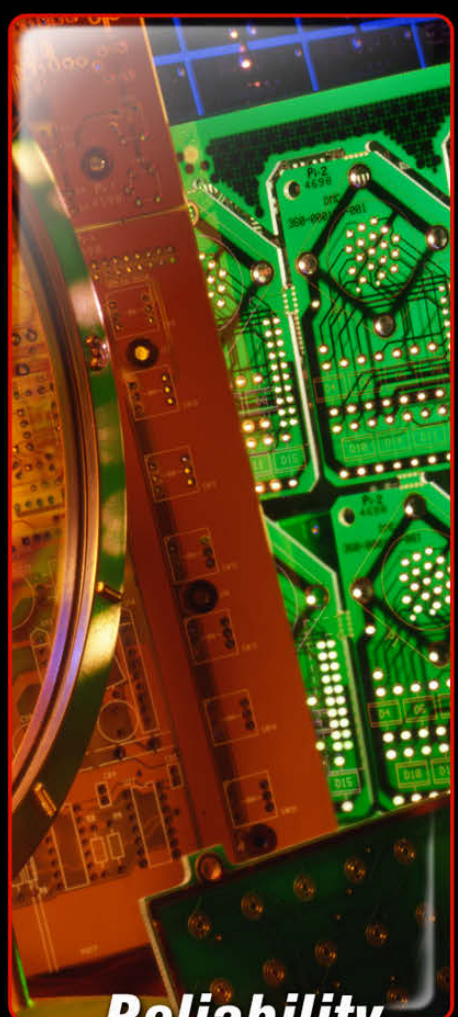

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is not yet well in that regard, that "hole" in the system is being addressed by businesses, NGOs and governments around the world.

Not to be forgotten is the fact that the impact of the EU's decision has been significant and far-reaching and it has caused the industry to spend needlessly many tens of billions of dollars diverting the considerable talents of countless talented engineers and scientists around the world to make products that are unfortunately proving less reliable and arguably less environmentally friendly electronics than those built with tin lead solders.

The Devil We Know, Disrobed

While soldering (especially tin-lead soldering) holds many benefits in terms of offering a means of mass assembly of electronic components to printed circuit boards and is fundamentally simple, its application in the assembly and manufacture of electronic products of the present age is much more complex and fraught with opportunity for defects to be generated, but it is also the a demon we have elected to live with, for as the old saying suggests that "Better is the devil we know." The devil we know is at least familiar and the simple truth is that humans are creatures of habit and most of us abhor change. There is a lingering question in the current situation? Is dealing with the devil we know on a daily basis really worth the price we are paying?

Following is a recitation of some of the many types of solder and solder-related defects that test and inspection is tasked with finding before a product reaches market. Bear in mind as these defects are recounted and reviewed that the cost of defects rises as a product moves further from the manufacturing line.

a) Opens: Opens are discontinuities generated in the soldering process that can be manifest in assembly in a number of ways. For example, a bent or lifted lead on a QFP component, missing solder ball on a BGA, insufficient solder on an LGA or the warpage of the component during the high-temperature, lead-free reflow process can all result in an open circuit.

b) Shorts: Solder shorts are bridges of solder between one or more component leads on an assembly. As component lead pitch continues to drop, the incidence of short circuits increases. Presently, the threshold of pain for most assembly is experienced when the lead pitch drops below 0.5 mm.

c) Insufficient Solder: Insufficient solder is a condition where the amount of solder in a solder joint is less than desired or specified contractually through industry specifications or customer requirements.

d) Excessive Solder: Excessive solder is obviously the opposite of the condition of insufficiency and is again measured against agreements. It also introduces a wild card because it is not what reliability testing is based on.

e) Solder Cracking: Solder cracking is an obvious concern as it could result in a latent open circuit condition. Good during product test before shipping but then failing in the field.

f) Tin Whiskers: Tin whiskers are small metal projections emanating from a solder joint. They can grow up to 15 mm long and given the fine pitch of today's components, they are a significant concern. There are also challenging because they are typically a latent defect that shows up unpredictably. Past research indicated that the addition of lead to tin solder alloys would mitigate the formation of whiskers; however, with the ban on lead in electronic solders the incidence of whiskers is on the rise.

g) Poor Wetting/Dewetting: Good wetting is manifest by the presence of uniform coat of solder on both the leads of the component and terminations of the printed circuit to which they are joined. In areas of poor wetting or dewetting the solder thins appreciably in areas leaving only a thin silvery sheen.

h) Voids: Voids are defect which are often difficult to detect without use of special equipment such as an X-ray apparatus. The challenge with voids is that they represent potential weakness in the solder joint owing to their inconsistent nature. Voids can be found both in through-hole and surface mount components. In the case of surface mount components the voids are often extremely small and are sometimes referred to as champagne voids.

i) Blowholes: A term applied to a phenomenon where a small hole is observed in a

solder joint. Typically, the defect is found to be the result of discontinuities in the plated through-hole wall, which may absorb flux and then explosively out gas during the soldering process.

j) Cold Solder Joints: Solder joints that did not form completely a good metallurgical bond. They are often the result of the joint receiving sufficient heat to cause complete melting and joining of the solder. Cold solder joints are often seen in cases where the component lead is connected to a large thermally conductive feature or element and insufficient heat is retained near the lead to assure a good solder joint. With lead-free solders, the phenomenon provides a greater challenge as the amount of heat which must be supplied is much greater than it might have been with a tin lead solder, thus potentially degrading device and assembly reliability.

k) Brittle Solder Joints: Solder joints wherein the alloy formed in the soldering process due to dissolution of elements within the finish or on the circuit board (e.g., gold), results in a solder joint that is less ductile than the solder used in the assembly process.

l) Head-on-Pillow: A new type of defect which was identified only with the introduction of lead-free soldering. It is an unsettling type of defect in that it is not easily detected but could result in an intermittent open in the operation of the assembly. The term was chosen because the phenomenon is reminiscent of an individual's head forming a depression on a pillow.

m) Graping: Another lead-free related defect wherein the small, often ball-like particles of solder in a solder paste do not reflow completely, leaving a surface that looks like the surface of a bunch of grapes. Like head-in-pillow, it is a defect that may not be easily detected.

n) Tombstoning: Tombstoning is a term that has been applied to the appearance of a defect related to discrete devices such as resistors and capacitors, wherein solder connections are not made simultaneously; the slight lag causes the first side to reflow to pull back and rotate up, resembling a grave marker (which is somewhat apropos given that the assembly will likely be dead if tombstones are present).

o) Component Cracking: Component cracking can have multiple causes, one being a situation where there is a significant mismatch in terms of coefficient of thermal expansion between the component and the printed circuit to which it is attached. It can also occur if the assembly is flexed in the area of the component, causing the device to crack.

> ***"Component cracking can have multiple causes, one being a situation where there is a significant mismatch in terms of coefficient of thermal expansion between the component and the printed circuit to which it is attached."***

p) Popcorning: Popcorning is a phenomenon manifest when moisture entrapped within a component outgases during assembly, causing a blister to form in the encapsulation material. With the advent of lead-free soldering and its higher temperatures, the incidence of popcorning rises and in fact moisture sensitivity levels of components are degraded to reflect the new reality.

q) Solder Balling: Solder balling is a condition which happens during the reflow of a solder paste on a surface mount assembly. It is a result of the high temperature of reflow causing rapid volatility station of the flux and spatter of the solder particles that are part of the flux. While a viable solder joint may be created even as solder balls are being formed, they represent a risk to the long term reliability of the assembly as potential shorting elements.

r) Misregistration: Components with fine pitch leads, if jostled before or during the assembly, may be misregistered relative to the land pattern, resulting in a nonfunctional product.

s) Insufficient Cleaning Under Devices: As mentioned previously, insufficient cleaning under surface mount devices can result in latent failure through the formation of high resistance shorts or the growth of dendrites.

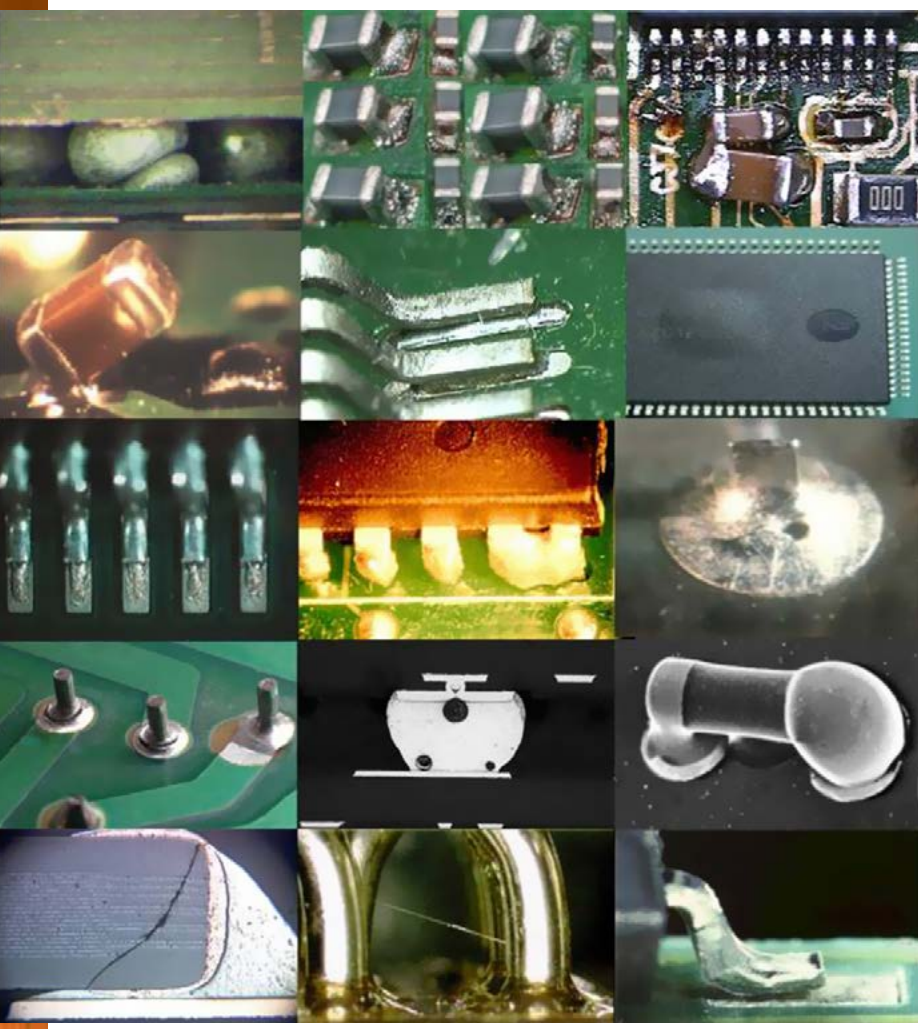

Figure 1: Representative images of some of the solder related defect found on printed circuit assemblies. Top row – left to right: head in pillow, graping, misregistration short and overheated flux. Second row, left to right: tombstoning, insufficient solder with open, popcorning. Third row, left to right: dewetting, blowhole, shorting between adjacent leads. Fourth row, left to right: cracked solder joints, voids, excessive solder. Bottom row, left to right: cracked component, tin whisker, open (lifted lead).

Clearly there is a great deal of nuance in the detection and identification of solder related defects; numerous books have been written over the last few decades that both characterize and suggest methods for eliminating or mitigating them (the devil is also "in the details" as another aphorism attests). It is not within the scope of this brief commentary to provide detail on all of the various types of solder related defects which can extend from the macro to the micro but for the benefit of the reader the following figure is offered providing representative examples of a number of the defects described above.

The "Devil's" Impact on the PCB

The importance of managing the soldering process is clear, but making a good solder joint is also just part of the story and there are a number of defects that can be generated within a printed circuit assembly because of the soldering process, including:

a) Corner Cracking: A crack that forms at the interface between the whole and the land that surrounds. It is normally the result of the Z-axis expansion of the PCB during the thermal excursions such as soldering.

b) Barrel Cracking: Another phenomenon associated with the soldering process; it is similar in some ways to a corner crack except that it is manifest near the center of the hole.

c) Post Separation: A separation of the plating in the through hole from an innerlayer connection

d) Hole-Wall Pull Away: Hole-wall pull away is manifest as a bulge in a plated through hole, which reduces its diameter.

e) Resin Recession: Roughly, the opposite of hole-wall pull away wherein a small gap is formed between the plated hole wall and a resin rich area of a plated through-hole

f) Delamination: A separation of the layers of a multilayer circuit. It is normally seen in cases where the glass transition temperature of the resins used in the multilayer structure is exceeded.

g) Pad Cratering: Another phenomenon unseen before the introduction of lead-free sol-

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dering. It is manifest as a circumferential tear of the copper land to which a component, normally a BGA, is assembled.

h) Decomposition: Decomposition of a PCB is a relatively new phenomenon associated with higher temperatures used with lead-free soldering. In fact, a new term was added to the industry lexicon, T_d, which is the temperature of decomposition representing a loss of a specified percentage of the weight of the printed circuit.

Clearly, printed circuit technology, like soldering technology, is fraught with its own vulnerabilities due to the complexities of processing. The demands on PCB technology foisted upon the industry by the imposition of lead-free soldering requirements have placed a heavy burden on the printed circuit manufacturing industry. The need for higher glass transition temperatures to assure a measure of survival through the elevated temperatures of lead-free soldering has required the printed circuit industry to qualify new materials. Simultaneously, there has been a demand placed upon the industry to remove halogenated flame retardants from its materials. This double-barreled challenge is one that the industry had not faced before. Moreover, the industry has been challenged to provide circuits with ever-finer features which operate at ever-increasing frequencies.

To their credit, printed circuit industry technologist, engineers and scientists have struggled admirably to address these challenges, including the challenge of finding solutions to defect modalities that were unknown to the industry just a few years ago. Unfortunately, a number of the defects described are related to soldering and its effects. The earlier problems have been exacerbated by the increased temperature required for lead-free soldering. Figure 2 offers cross-sections of representative printed circuit defects resulting from thermal excursions.

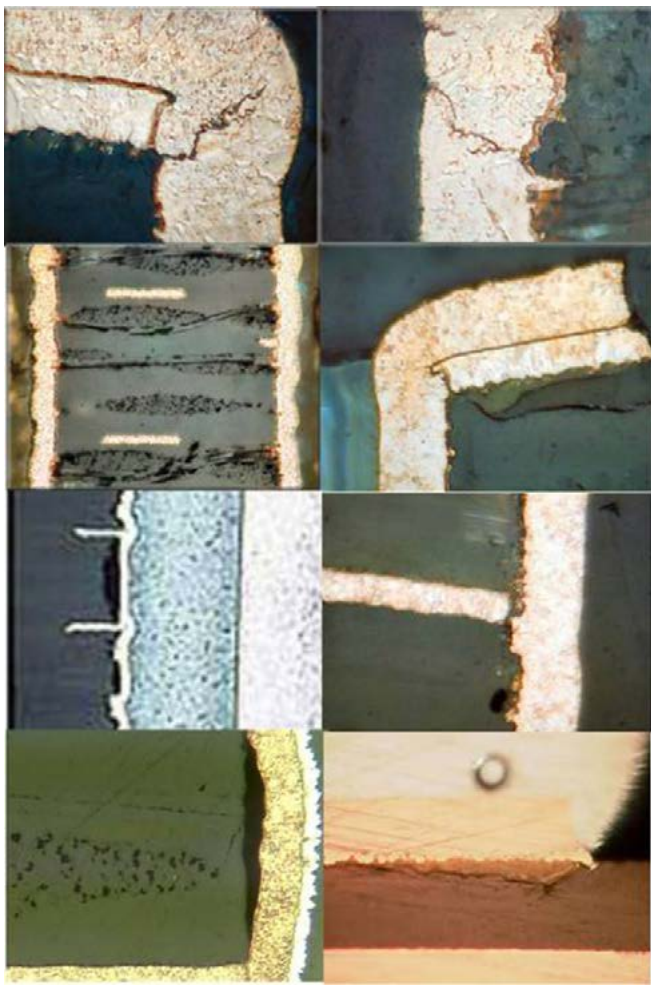

Figure 2: Cross-sectional micrographs of printed circuit defects caused by soldering are provided above. Clockwise from the upper left-hand corner: corner crack, barrel crack , pad lifting, post separation, pad cratering ,hole wall pull away, resin recession and delamination.

Solderless Assembly for Electronics (SAFE) Technology: A Simpler Approach?

Given all the challenges and risks associated with soldering, every thoughtful and prudent manufacturing engineer must constantly be seeking a way or ways to make assembly processing more robust. If one looks for inspiration on how they might end their dealing with the devil, they can find it in the Bible, where it is written: "If thine eye offend thee, pluck it out, and cast it from thee." Perhaps this is a bit extreme, but this seems to be where the industry is stuck today in dealing with the devil. Solder is by analogy an offending element of manufacturing and source of many if not most manufacturing problems. The industry will continue to have to deal with that devil as long as we persist in its use.

One can do their own research to test this assertion if they choose. They need look no fur-

ther than the titles of papers in publications. Presently, this and other industry/academic journals and proceedings on electronic manufacturing are rife with articles, papers, commentaries and advertisements offering new materials, processes and equipment both for manufacture and inspection to try and beat lead-free solder into submission. Unfortunately, solder appears a wily and crafty adversary that always seems to offer another challenge to each new solution proposed. This situation begs the question: "Is there any alternative?" The answer, in the opinion of this author, is "Yes." The answer is to assemble electronics without solder.

The potential benefits of eliminating solder is significant in many areas of current concern or high interest in electronic manufacturing, including: cost , reliability, performance, environmental impact, design security, a means of addressing some elements of counterfeiting, sustainability, a means of sidestepping conflict metals concerns and others.

So how can it be done? It is really quite simple: Build assemblies in reverse and instead of placing and joining components on circuit boards with solder, build up circuits on "component boards" using copper plating, thereby bypassing the soldering process completely along with all of its many extra processing steps, ongoing challenges, and problems. The potential economic, environmental and reliability benefits are substantial as will be shown. The concept of SAFE assembly and its practicality will be examined in more detail in a future paper. **PCB**

Verdant Electronics Founder and President Joseph (Joe) Fjelstad is a four-decade veteran of the electronics industry and an international authority and innovator in the field of electronic interconnection and packaging technologies. Fjelstad has more than 250 U.S. and international patents issued or pending and is the author of Flexible Circuit Technology.

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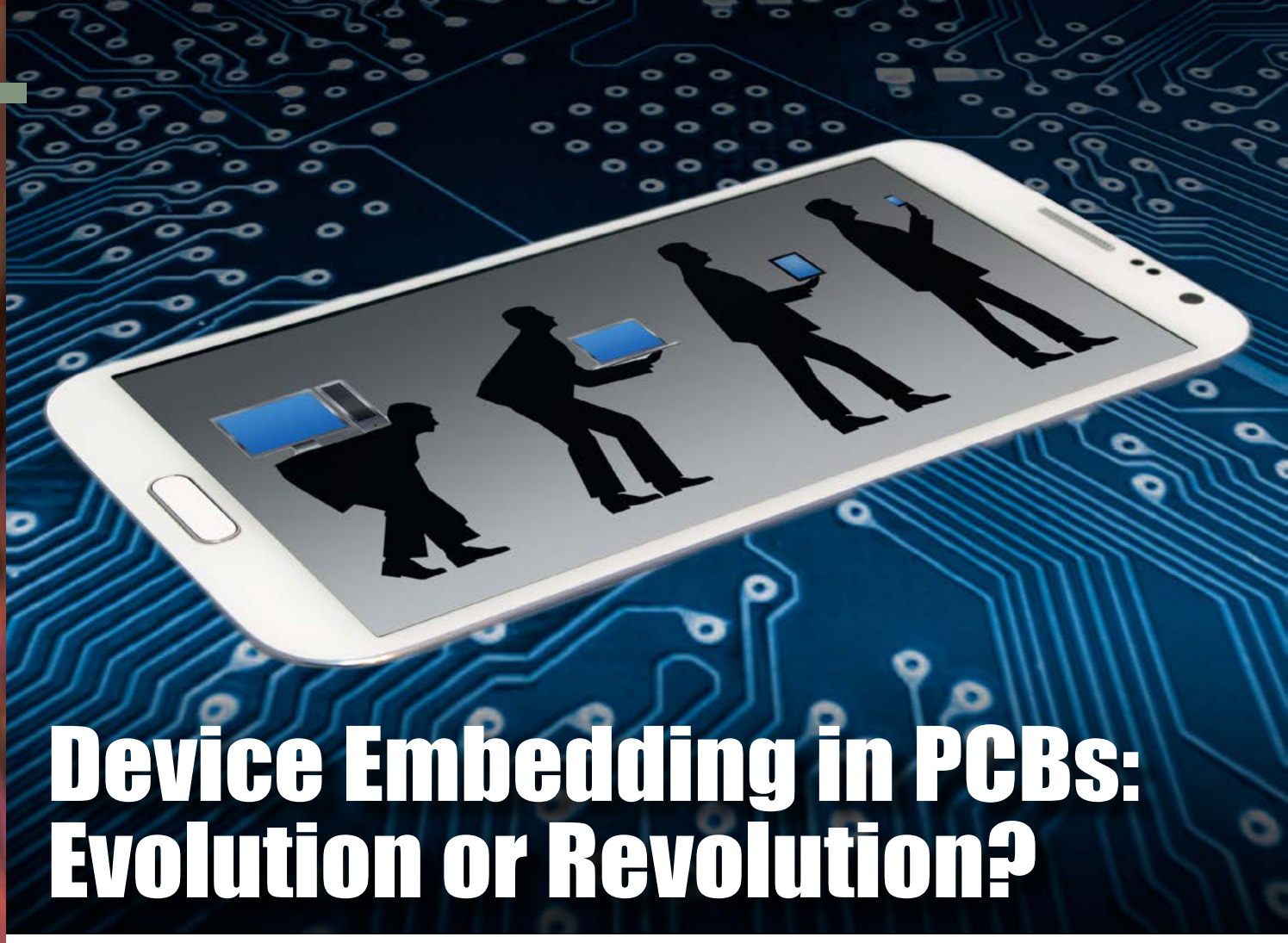

Device Embedding in PCBs: Evolution or Revolution?

by Michael Weinhold
EIPC TECHNICAL DIRECTOR

Abstract

The embedding of components in electronic interconnection structures has been carried out for more than 30 years, and while different technologies have developed and were technically successful, history has shown that these embedding developments did not result in a sustainable success over a longer period of time. Replacement technologies have been developed after a short period of time by the so-called "Not in Kind" (NiK) technologies (e.g., inorganic = not in kind, organic = in kind).

This article will explain what is needed to avoid technology pitfalls that lead to future business failures.

In addition, opportunities are discussed that enable development managers, design engineers and specialists to use the full benefits of embedding devices in automotive, medical and industrial applications. These enabling manufacturing technologies will offer the opportunity to develop innovative product solutions in critical technical, environmental and business situations.

Introduction

The number of PCB fabricators in Europe has declined over the last 20 years to less than 25% of what it was at the end of the 1980s. Today, Europe has little more than 250 PCB fabricators with a turnover of about US$2.7 billion[1]. Large companies like Siemens, Philips, Alcatel and IBM closed their in-house PCB manufacturing plants long ago. For the remaining PCB companies in Europe the strategy is more focused on survival, with growth as a near-goal objective. Under these circumstances, innovation is a major part of the survival strategy. To stay in business today, it is important to understand what field of business the company is operating in and what are the means necessary to differentiate your company from other suppliers, wher-

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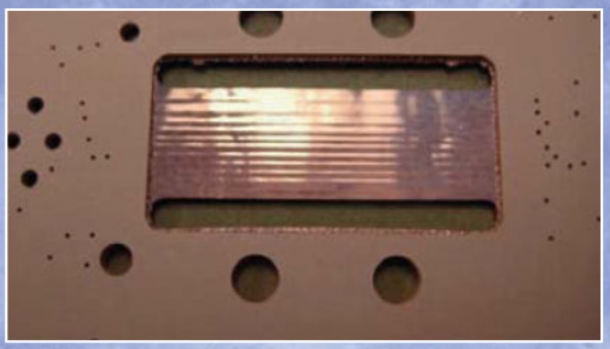

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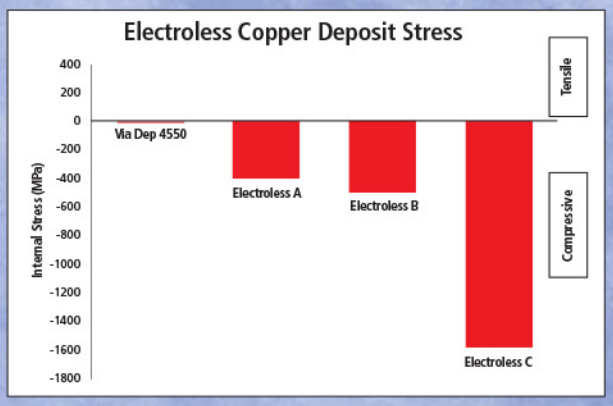

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ever they may be. The PCB fabrication market was a suppliers market in the '80s. The supplier (i.e., the PCB fabricator) could set the prices for his products and the customer had to agree on it to get the products. Today, the PCB market is a buyer or purchasing agent market. The prices for PCBs are, in many instances, defined by the product buyer. Often, the PCB fabricator has no option but to agree to the offered price or he will not get the order. Furthermore, in longer-term contracts, price reductions are included—often between 5–10% p.a. Purchasing agents are using the well written IPC standards to define the workmanship and the quality of the finished PCBs. On many occasions these requirements are over-specified and do not reflect the required manufacturing technology and tolerances needed for a given application. PCB fabricators have to learn again that they are in the business to make money and that the PCBs are the tools to achieve this task. In addition, the PCB purchasing agents or buyers have to learn that only a PCB fabricator that makes money will be able to stay in business and will have the financial resources to invest in future technology, innovation, manpower and equipment.

Embedded Technology in Europe

Why use device embedding in PCBs?

Device embedding technology in Europe is used to add electronic, mechanical, thermal management and environmental function to PCBs as well as increasing the value to the basic PCB. For PCB fabricators, component embedding means leading integration in the supply chain. It will also shift the focus away from the PCB assembler to the bare board PCB fabricator who embeds the devices in the PCB.

Historical development of device embedding in PCBs

Embedded passive components have been used in large quantities in ceramic hybrid circuit fabrication since the '70s. Active components have been wire bonded, soldered or glued to such modules. In the late '90s, component embedded technologies using organic PCB materials were patented by Hofmann Leiterplatten GmbH for the AML technology[2] and by SIEMENS AG in Germany for SIMOVE® technology.

The SIMOVE (Figure 1) technology was very successful for a period of 2–3 years[3]. Licenses

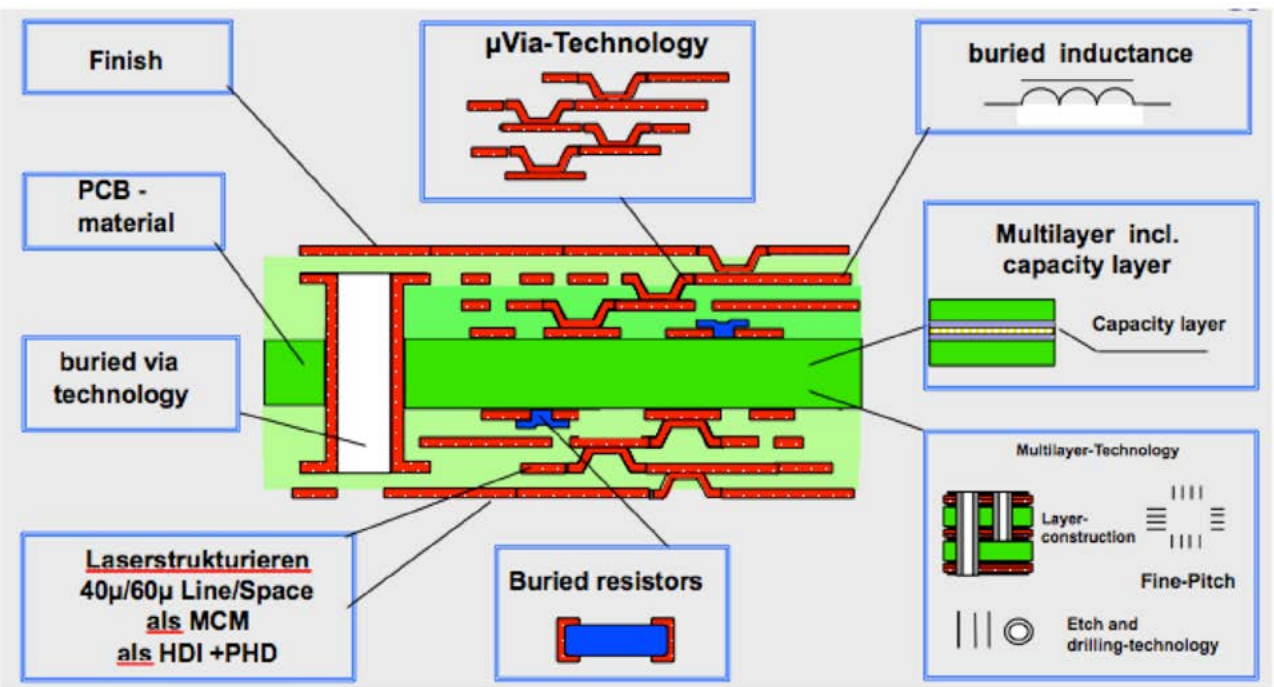

Figure 1: Technology options used in the SIMOVE technology developed by SIEMENS AG in Germany[3].

have been given to the PCB fabricator industry in Europe, necessary to overcome the issue of a single source supply chain. At the end of the '90s, the PCB industry was anticipating a growing business from this newly-developed SIMOVE[3] technology. So it was a big surprise that this investment did not result in additional business; indeed it was quite the opposite. At the moment the SIMOVE technology was ready for industrialisation, it was no longer needed. The reason was that the integration on silicon was so much advanced in functionality and cost-reduction that the embedding design—using PCB technology—did not offer any packaging or cost benefits.

The questions that need to be answered are:

- Is there a market for embedded devices in PCBs in Europe or in the market worldwide?
- Under what circumstances could the PCB fabricator benefit from these markets or market niches?

To answer these questions we must look at the changes in the market and in the demand by key OEMs and industry segments.

Semiconductors Drive Electronic Design

In the electronics business it is important to understand that the semiconductor suppliers are much larger than PCB suppliers. The top 25 semiconductor fabricators (Figure 2) have a turnover of about 4 times the total global PCB market with more than 1500 fabricators worldwide.

As can be seen, the semiconductor market is no longer a fast growing market. The semiconductor industry is looking into opportunities in forward integration in packaging, like SiP (system in package) or even in SiPCB (system in printed circuit boards). When the quantities are large, the design on silicon is one option to expand the business.

An additional example was experienced at the beginning of the smartphone era. Flip phones with many PCBs and flex rigid board combinations with integrated key boards were acclaimed as the solution for the future. Optimisation technologies with special rigid-flex PCB designs offered an excellent technical solution and generated more business for the PCB industry.

At this point, the semiconductor fabricators recognised the quantities needed in future for

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Total Top 25 represent 234,232 -1%

Rank	Maker	2012	2012/2011
1	Intel	49,114	-1%
2	Samsung Electronics	32,251	-4%
3	TSMC	17,167	18%
4	Qualcomm	13,177	34%
5	Texas Instruments	12,147	-6%
6	Toshiba	11,217	-12%
7	Renesas	9,314	-13%
8	SK Hynix	9,057	-4%
9	STMicroelectronics	8,364	-13%
10	Micron	8,002	-7%
11	Broadcom	7,793	9%
12	Sony	5,709	-6%
13	AMD	5,422	-17%

Rank	Maker	2012	2012/2011
14	Infineon	4,993	-11%
15	GlobalFoundries	4,560	31%
16	Nvidia	4,229	7%
17	Fujitsu	4,162	-6%
18	NXP	4,157	0%
19	Freescale	3,735	-15%
20	UMC	3,730	-1%
21	MediaTek	3,366	13%
22	Sharp	3,304	14%
23	Marvell	3,157	-8%
24	Elpida	3,075	-21%
25	Rohm	3,030	-8%

Figure 2: The top global 25 semiconductor leaders represent 4x the total global production of PCBs[4].

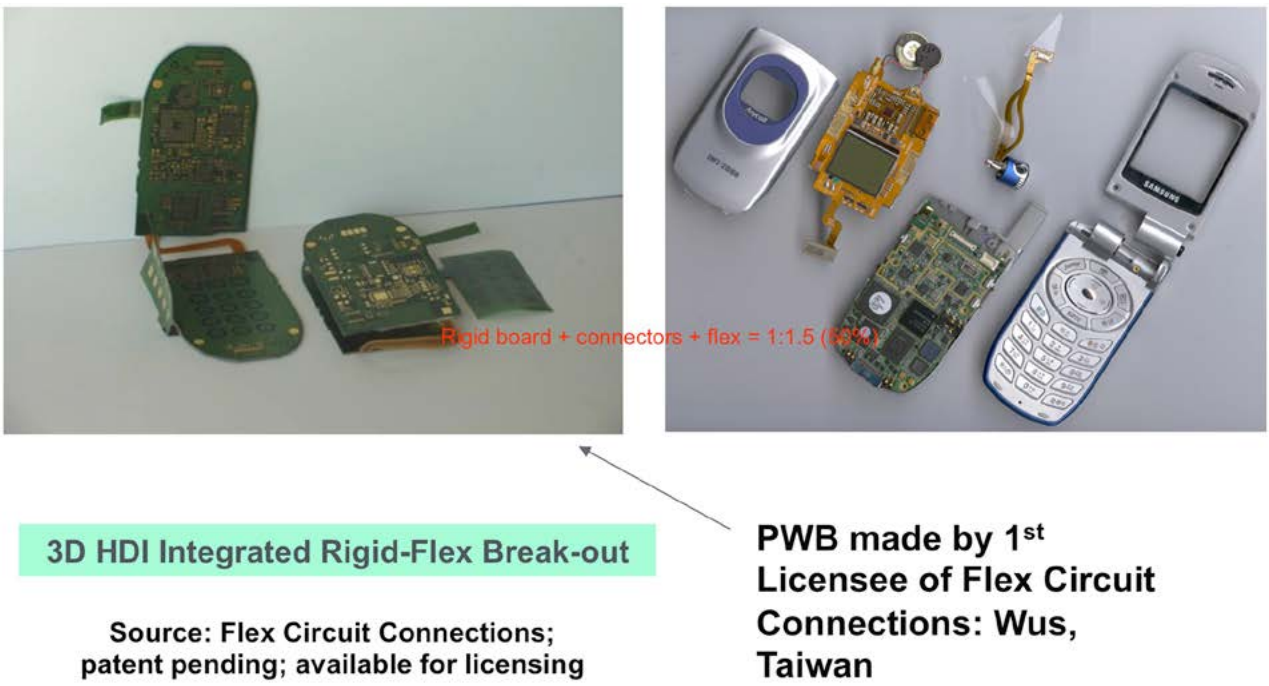

Figure 3: Traditional flex vs. 3D HDI integrated rigid-flex breakout V 1.1[5].

Figure 4: Smartphone technology evolution. No keypad, no flip screen. Three keys, but a high definition touch screen that offers many more benefits compared to a conventional keyboard[6].

these advanced mobile communication tools. In addition, smartphones become even smarter and more electronic functions were essential to meet the growing consumer hunger for new features. Video phoning, video games and television became standard requirements, besides making phone calls and sending e-mail, SMS and MMS messages.

Today, smartphones without keyboards fulfill the function of communication tool, television, video player and videophone as well as a radio and music centre and, in some cases, they even replace computers.

When manufacturing such electronic devices, intelligent component packaging is the solution. Semiconductor fabricators can integrate these functions into a semiconductor package or even design it direct onto silicon. For the mobile phone, where the quantities are in the tens of millions, the required investment for these electronic devices can be easily justified. In the field of automotive applications, where quantities are smaller (< 10 million) the design on silicon may not be the solution. Here, the fixed costs of designing a customized chip, including the interfaces and the related software, are very high in relation to the quantities needed. However, when system-in-package and system-in-PCBs are more widely designed and accepted, this situation is more cost-effective and this will change how car electronics are designed and manufactured in future. New opportunities for interfaces between devices may apply in near field communication (NFC) protocols, may re-

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place connectors and flexible PCBs, and may even change the automotive assembly technology. In addition, RFID components have become cost-effective alternatives to store important information about the assembly processes and environmental requirements and other unique device information. This technology will offer even more options for the software developers and system designers of the future.

Advanced Projects in Europe

Europe is strong in automotive, industrial, medical, photovoltaic, avionics and space electronics. In addition, power electronic devices are needed in many of the new electronic automotive application. As indicated in the beginning of the report, the PCB market is at present a buyers' market and the purchasing managers and/or agents define where the order is placed. For them, cost reduction is one of the key objectives, but will, in many cases, not go in line with innovation, reliability, traceability and environmental requirements.

The European industry depends on leadership through innovation in electronics. Compromises between cost-reduction and innovation are key drivers for the PCB fabricators and OEM/EMS industry in Europe. Today, PCB costs are calculated on a square meter or square decimeter level. The smaller the PC board, the lower the selling price for it will be.

One example is the EU-sponsored consortium project "HERMES" (High density integration by Embedding chips for Reduced size Modules and Electronic Systems). The following companies have cooperated as partners: AT&S Austria Technologie & Systemtechnik AG, Atotech, Bosch, Circuit Foil, Fraunhofer IMZ, IMec, Infineon, Rood Microtec, Siemens A&D, Thales Communications France (Thales

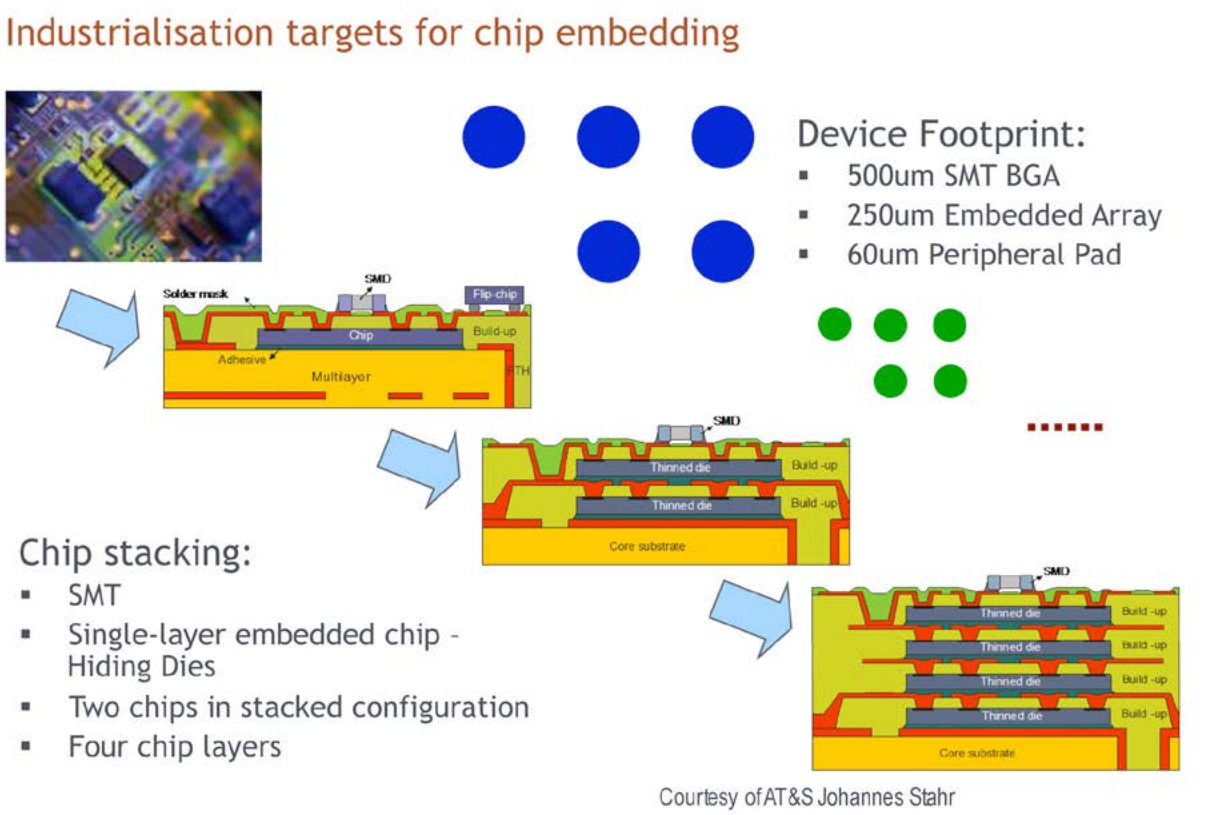

Figure 5: Project supported by the European Commission under the name HERMES. Industrialisation was carried out at AT&S in Austria together with Fraunhofer IZM in Berlin. The project partners came from the fields of acadæmia, OEMs, silicon fabricators, and the chemical, electro-plating and packaging industries[7].

TCF) and Thales Corporate Services. This project resulted in a successful product development for a new technology, which is now used in Europe to manufacture several million units per month. In this project, the benefits of PCB technology have been modified in a way that it is fully functional in the area of cost-effective chip packaging fabrication.

In this project, the chip-in-polymer process has been developed and industrialised, which offers a reliable and cost-effective embedding technology for the realisation of modules and SiP development. This technology is applied in several projects with industry and R&D centers.

The industrialization of the technology within the "HERMES" project was a great achievement for the electronics industry in Europe. Without funding from the EU the partners would not have seen sufficient benefits and incentives to develop these new packaging technologies. The package realisation resulted in single and multi-die packages and provided a reliable and cost-effective solution compared in compared to conventional IC packages.

The HERMES project was direct application-related and resulted in multiple levels of embedded chips, multiple lamination cycles, embedding of ultra-thin chips in flex, power modules and radar applications of 77 GHz.

The products that have been developed under this project are not easy to copy. Special investments are needed to perform the required technologies and co-operation between PCB fabricator, assemblers and chip fabricators are needed to get the required unpackaged components. At present, most of these products are manufactured in Europe.

Experience has proved that the European electronics industry very much depends on innovation. Based on such by the electronics industry, the Active Multi Layer (AML®) technology was developed by Hofmann Leiterplatten GmbH in Germany. The goal was to combine the benefits of the standard copper clad laminate, prepregs and epoxy resin as well as standard placement and soldering technology into one embedded device with an advanced thermal conductivity of these materials in one package. The key to success is based on using standard materials (Figure 9), assembly attachment and soldering processes in conjunction with some modified standard manufacturing PCB processes. Key in the success of this technology is the control of the design, the PCB fabrication and assembly processes. Today, standard PCB fabricators do not have these capabilities. However,

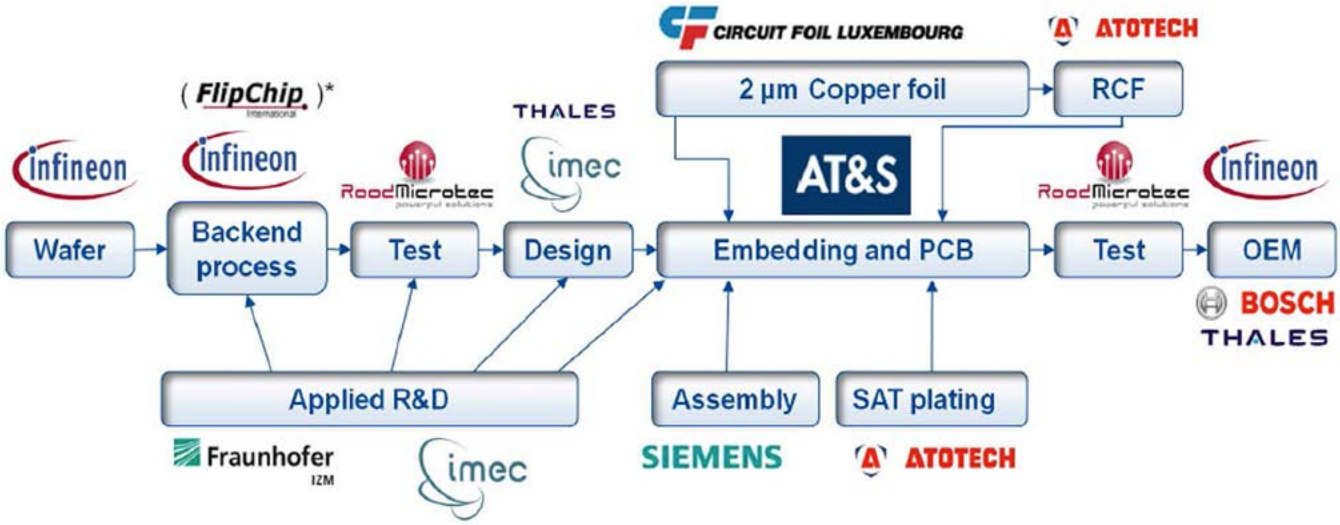

Figure 6: The success of the HERMES project was based on the involvement of the total supply chain for electronic devices. Representatives from silicon wafer fabrication, materials and process suppliers, to packaging to end-users with specific applications proved the need for this form of package and product[8].

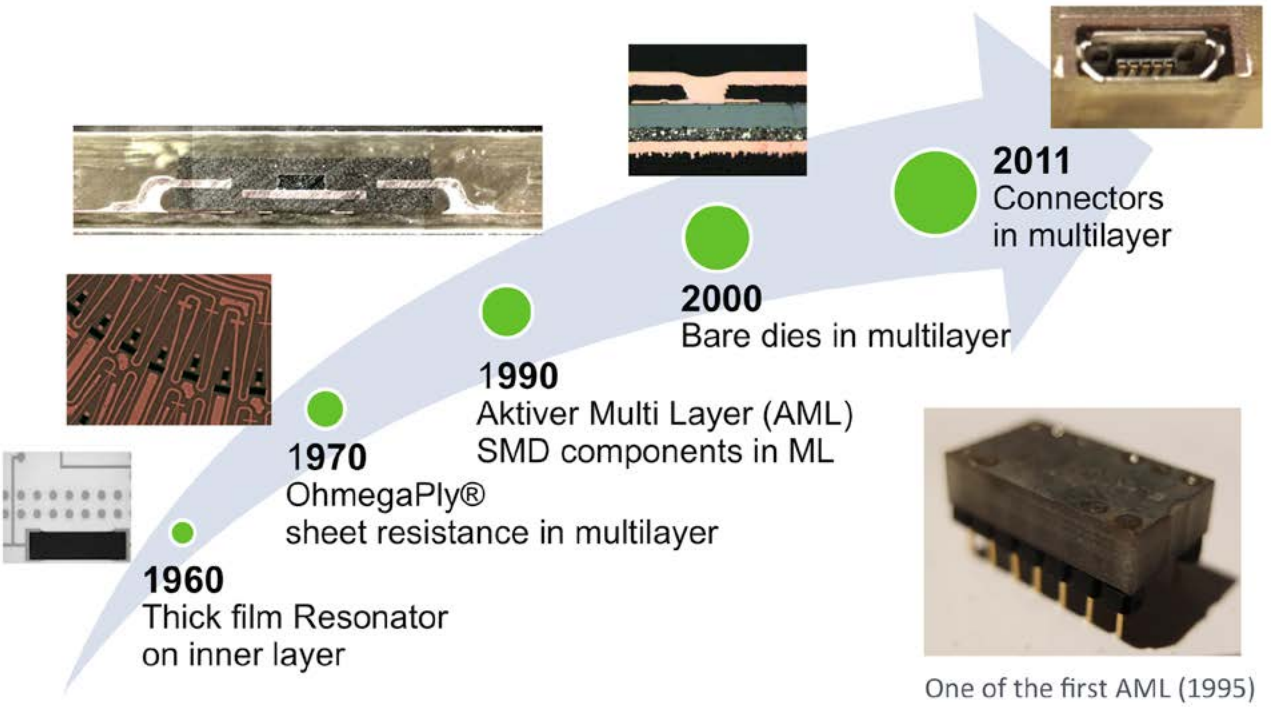

Figure 7: Device embedded technology in PCBs using standard packaged components. Active multilayer (AML®) technology developed by Hofmann Leiterplatten in Germany can use standard components including connectors inside the PCB. Miniaturisation, reliability and improved thermal management are achieved simultaneously[2].

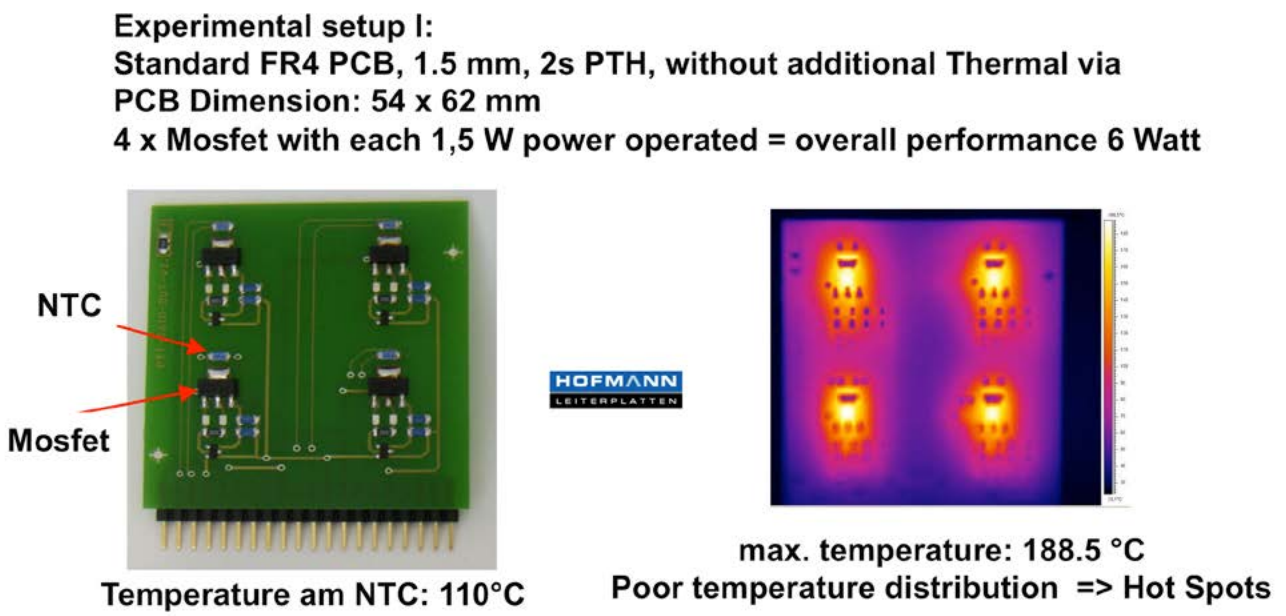

Figure 8: Mosfet components on standard assembled PCBs can generate high temperature, as cooling is only by ambient air which has low thermal conductivity[2].

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In the experiment, standard PCBs where assembled with four Mosfet components powered with 1.5 W. The PCBAs were operated for some time and then the surface temperature was measured. Using thermography measurement methods, the temperature showed hot spots of >188°C at the components. Even the thermosensor still showed a temperature of 110°C. Life expectation of electronic devices depends on the operating temperature of the components and the co-efficient of thermal expansion in X-Y and Z direction. Operating an electronic device at a lower temperature will increase the life expectancy or the mean time between failures (MTBF).

Material	Thermal Conductivity in W(m/K)
Acrylic	0.2
Air	0.024
Aluminum	250
Copper	400
Epoxy	0.35
Glass	1.05
PTFE	0.25
Silicon	149
Water	0.58

Figure 9: The thermal conductivity of different materials used in PCBs indicate that air is not the prefered media when thermal disipation is required. Epoxy resin has a 0.35 W(m/K) thermal conductivity and glass has 1.05 W(m/K)[9].

Repeating this experiment with the same layout, the same type of components and same manufacturing technology was used to embed the components inside the PCBs. In this process, the components are completely surrounded by epoxy resin and glass fibres used in copper clad laminate and prepregs. A dramatic temperature drop at the component was achieved. As shown in Figure 10, the thermal conductivity of the base material indicated no hot spots on the

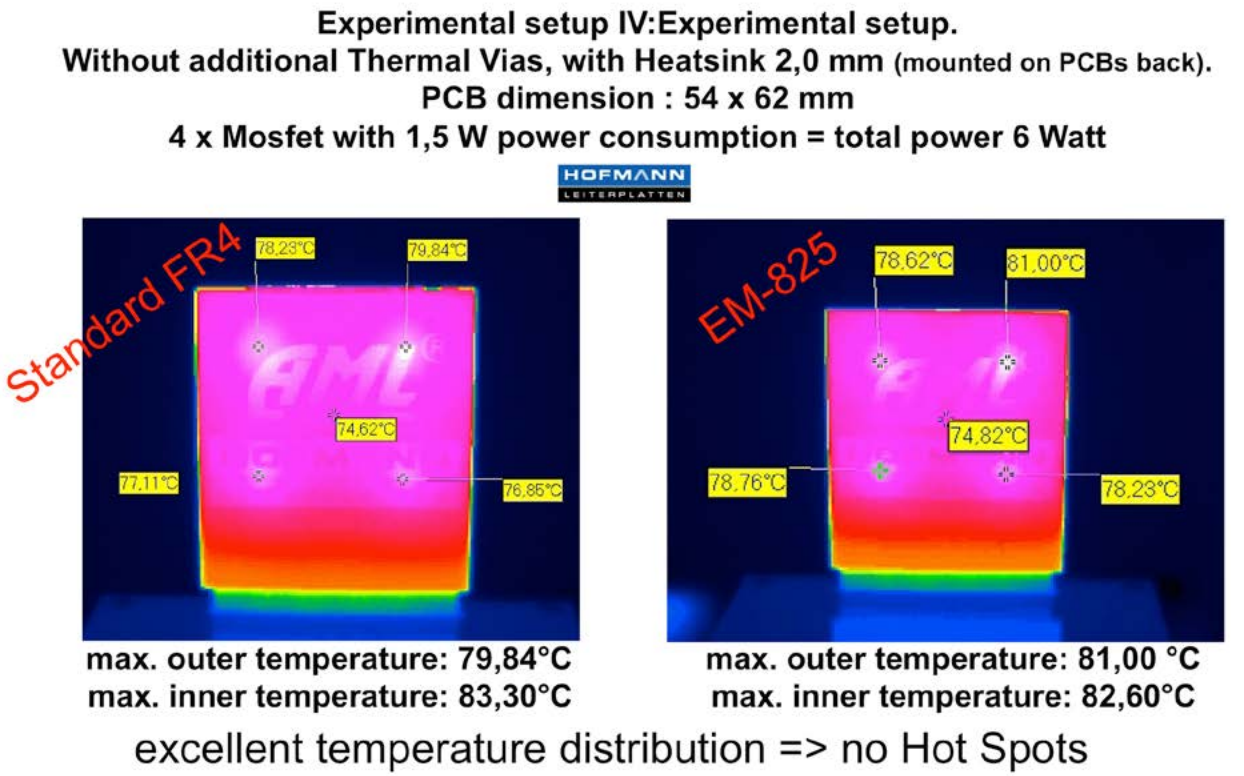

Figure 10: Components embedded inside the PCB assembly have shown much lower temperatures based on better thermal conductivity of CCL compaired to air[2].

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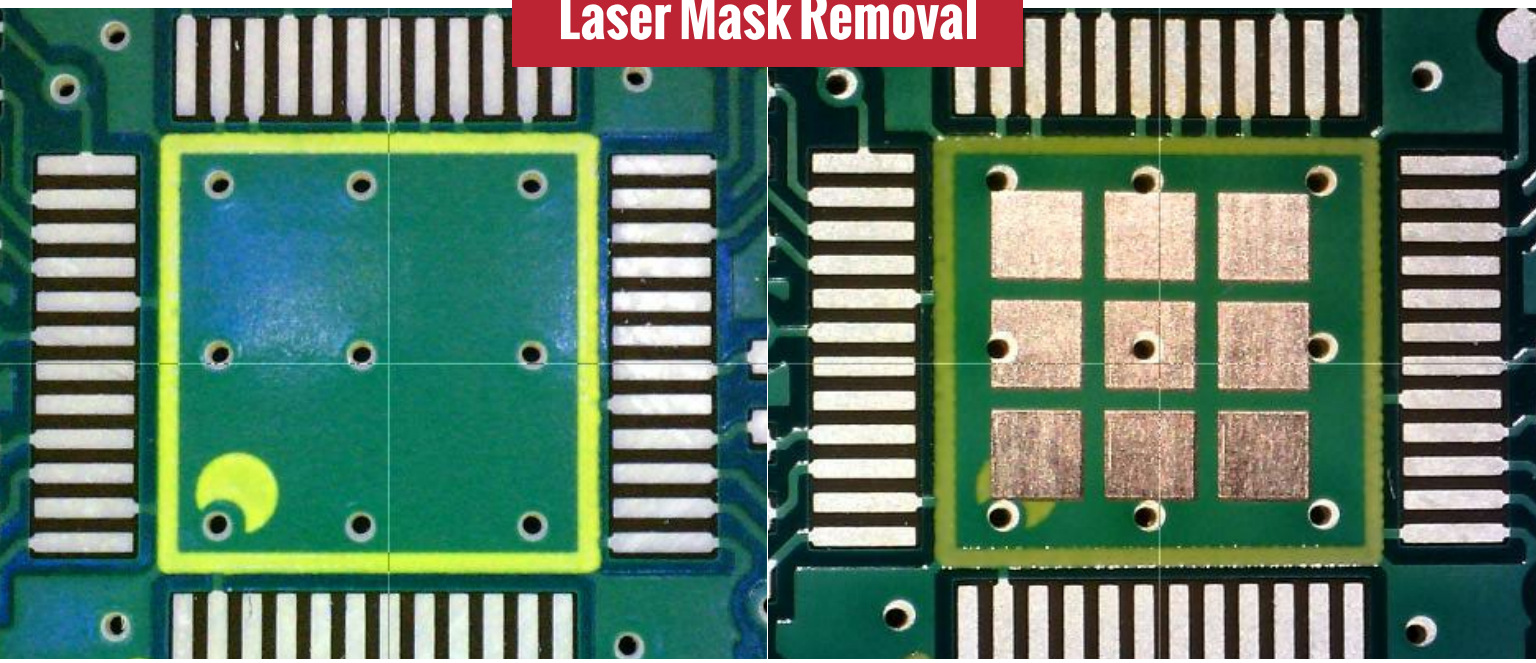

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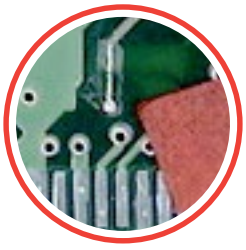

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PCB. The total PCB temperature is lower, not only at the components.

It is expected that the PCBs with embedded components are operated at a lower temperature. This will result in an extended operating life of the electronic device. An OEM and or EMS company can use this benefit to show a larger number of hours for the MTBF. This will be a reliability argument when it comes to product life expectation and will be, in many cases, a strong sales argument and it indicates a commitment to quality.

The component embedding technology offers an additional benefit in protection against environmental contamination, dust, humidity, gases and various chemicals. Encapsulating in epoxy resin can, under certain circumstances, replace housing, improve EMC shielding, help in miniaturisation and improve the thermal properties of the electronic devices.

Impact of European Commission on Embedded Innovation

To understand the opportunity for technical innovation, it is important to consider the markets the European industry in operating in. As countries operating under EU legal administration, it is important to adapt to the legal changes in Europe since the European Union was, in its present form, implemented in 1992[11].

The 24 official languages in the EU can make communication difficult, but although about 20% of the population in Europe speak German, it is widely recognised that English is the language of business[12].

In Europe, the German-speaking counties represent a large section of the industrial production and it is recommended to communicate in the local languages. This is very important at the new electronics development stage when new products are being designed. In addition it

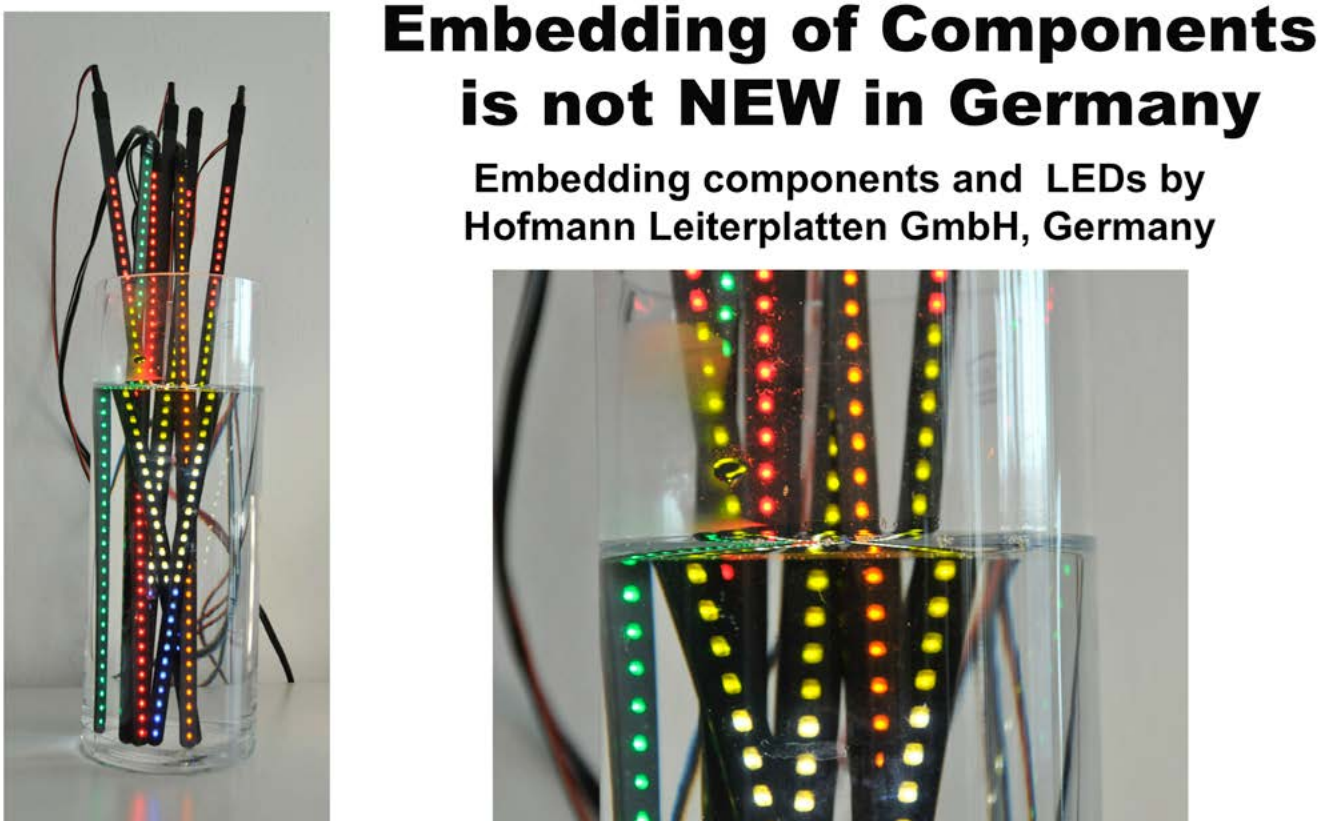

Figure 11: LEDs embedded in CCL survive exposure to chemicals and water/humidity very well. In this sample, the illuminated LED strips are partially in water for more than five years, without damage[2].

is important to understand that electronic designers in many cases are not the PCB designers. Printed circuit board designers do not know all the details required to design for manufacturing (DFM) and design for the end-use application where the final electronic device is used. To design for the best technical and most cost-effective solution, close cooperation in the supply chain is a major key for success. Here, a strong impact on cost is given by the fact that PCB solution can be manufactured locally during the development phase.

It is a common practice that prototype and small series of PCBs are sourced usually at local PCB fabricators (Figure 13). Here, good communications and technical know-how of the PCB fabricators are needed to manage an effective development cycle and to ensure that the electronic devices are working as specified. These development cycles have sometimes been seen as difficult, when language barriers and technological standards as well as different manufacturing standards are used. In the areas of industrial electronics, medical and avionics and space application, the quantities of PCBs that are required are small to medium. These run lengths can be cost-effectively manufactured in Europe. But when it comes to consumer electronics and automotive, the situation is different.

In the automotive field, much product development takes place in Europe, and therefore the prototype PCBs and the start-up production originates in Europe. When larger quantities of products are needed, and the PCB technical requirements are well covered by standards, low-cost manufacturing countries are chosen. However, when the demand for the required units gets larger, the in-kind PCB fabrication process may be changed against a not-in-kind (Figure 14). Therefore it is important to understand that different technical solutions can adopt different manufacturing technologies. These are the following options:

- Organic material solution (PCB)
- Ceramic material solution (LTCC)
- Silicon technology solution (SiS)

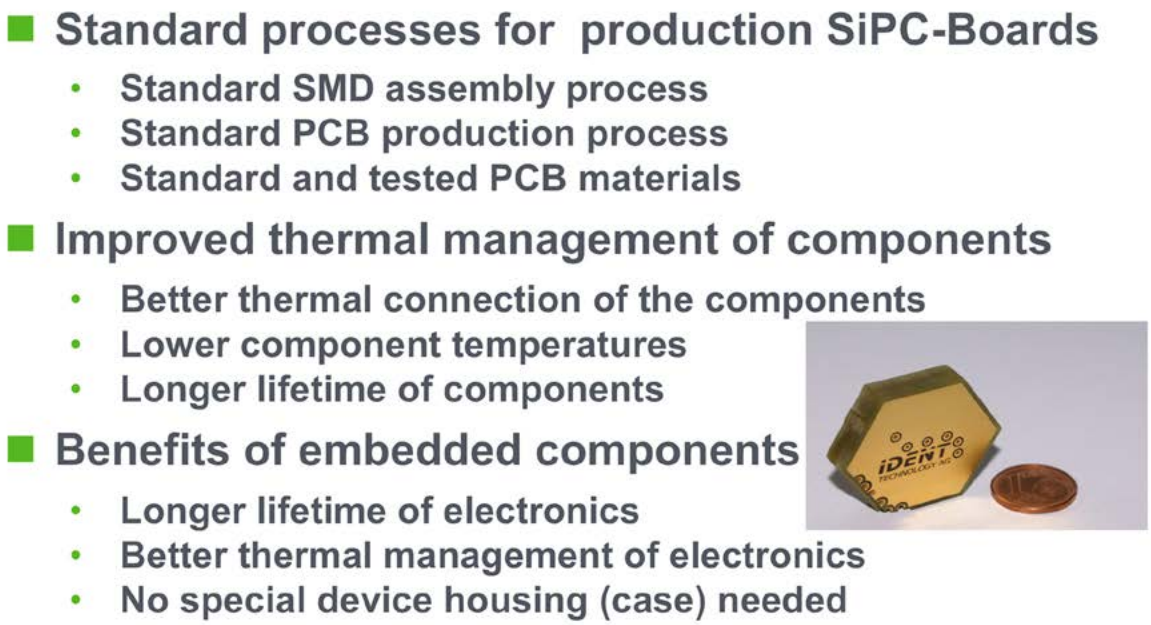

Figure 12: Proximity sensor with two assembled inner layers and 90 integrated SMDs. All of the parts were made using PCB manufacturing technology and materials and the applied process (AML) was developed by Hofmann Leiterplatten in Germany[2].

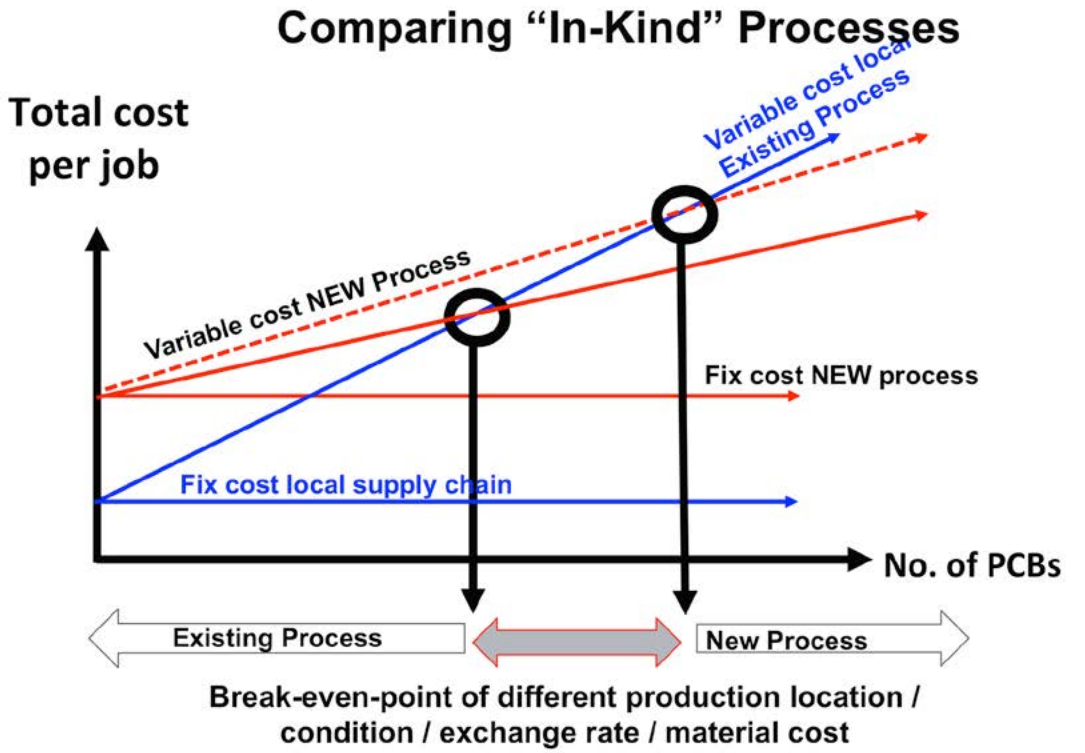

Figure 13: Small series of PCBs using an in-kind PCB technology are manufactured locally while large series are often sourced globally[10].

Summary and Outlook

New product developments require new ways to improve quality, miniaturisation, and efficiency, including energy efficiency, and in many cases improved thermal management. Device embedding technology in PCBs has a large potential to meet these future requirements. However, PCB fabricators have to learn how to absorb and master the technology challenges not only of fabrication, but also of assembly of device testing, and end use application.

In addition, PCB fabricators have to understand that the actual quantities of manufactured boards will determine the market opportunity for the printed circuit board technology. When quantities are large, as in the mobile phone or computer tablet business, the chip and the chip packaging industry will sooner or later work out a solution that takes this market segment away from the PCB technology (Figure 14).

Based on historical information from the hybrid circuits industry in the '80s and from organic embedded device technology (e.g., SIMOV) in the '90s, the PCB industry has to encourage electronic designers to focus on many new developments in technology. This will stimulate demand in the area of small to medium PCB quantities, and, based on the cost structure of the PCB fabrication process, the production of small batch sizes should offer a good return for the PCB fabricators. For the semiconductor industry the start-up fixed costs are too high to focus on a small number of products, and therefore these market segments are of little interest to the chip and the chip packaging industry. In addition, many new designs require good engineering at the PCB fabricator and a good communication between the development engineers. Both must exist to ensure success. **PCB**

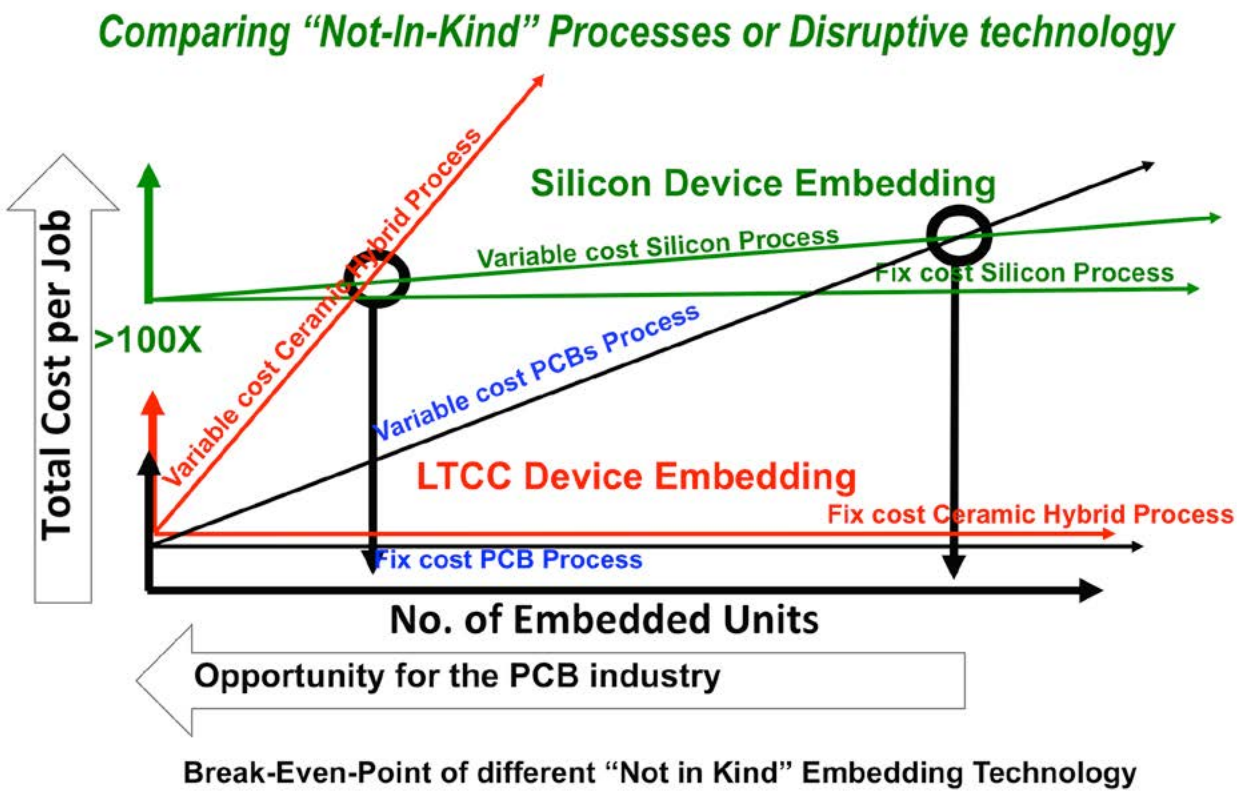

Figure 14: For large quantities, a not-in-kind technologies may offer technical as well as cost benefits. In addition dimensional changes and miniaturisation are also key drivers for alternative technologies[10].

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13. The European Union (EU) has more than 500 million inhabitants, who represent a large industrial and consumer market. The EU today has the third largest population after China and India.

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RF Capacitor Material for Use in PCBs

by Jin-Hyun Hwang, John Andresakis, Ethan Feinberg, Bob Carter, Yuji Kageyama, and Fujio Kuwako
OAK-MITSUI TECHNOLOGIES

Abstract

A novel ceramic-functional-particle-filled polymer composite material has been developed for the use either in discrete elements on the PCB or in being embedded within the packaging substrate for high-frequency circuit applications. This material provides the desired properties such as low loss at high frequencies (about 0.002 or less up to 10GHz) and high dielectric strength, among other improved properties. The electrical properties were influenced significantly by the ceramic-functional-particle (type and particle size/distribution in the polymer matrix). Their contributions to the electric strength and temperature stability of capacitance (which is an important material issue for practical device application) will be discussed. In addition, capacitance tolerance for manufacturing an embedded RF capacitor will be presented in terms of etching uniformity to minimize the variation of the capacitor electrode areas.

I. Introduction

Organic-based dielectric materials has been explored for the use either in discrete passive components on the PCB or in being embedded within the packaging substrate as part of RF/microwave circuits[1–4]. Using ceramic-functional-particles (fillers), filled polymer composite material is merely a convenient and inexpensive way (to compete with ceramic chip capacitors) achieving low ESR (equivalent series resistance), high SRF (self-resonant frequency) for RF capacitor application that can support frequencies well above 1GHz. Besides, embedding fillers into the polymer enhances properties of dielectric materials (by optimizing filler chemistry and its distribution in the polymer matrix) such as temperature stability of capacitance for high precision RF circuit and dielectric strength (the

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maximum DC electric field strength applied across the dielectrics in RF capacitor) for a high voltage rating which is essential especially for servers, pico cell and femto cell in base station market space. Generally, fillers are widely accepted in various applications because of their advantage in addressing several limitations of polymers, making its way onto benefits such as better dimensional stability for polymer composite membrane, lower coefficient of thermal expansion (CTE) for build-up layer, increasing thermal conductivity for thermal interface materials (TIM), and improved stiffness for underfill materials. As for the fillers in RF capacitor application, it is presently based almost entirely on the simple perovskite $BaTiO_3$ (barium titanate), but there is strong demand on the class of materials known as paraelectrics, mainly due to the fact that their dielectric properties are much more stable with regard to most operating conditions such as frequency, temperature and DC bias[5].

Well-dispersed fillers in polymer composite matrix play a crucial role in achieving RF capacitor requirements as described above and thus factors that determine fillers distribution should be controlled and optimized. Any existence in the particle agglomerates is accompanied by the formation of possible defects such as trapped porosity that make the dielectrics vulnerable under practical operating conditions. Figure 1 shows typical example of severe filler agglomerates clearly visible, concentrated on the coating surface as discrete protuberances and appearing to be in greater numbers. Filler agglomeration is easy to observe by improper usage of dispersion agents and their mismatching to a solvent composition in formulation. It could degrade electrical properties, in particular dielectric strength and temperature stability of capacitance (both will be described in next section). Various types of coupling agents can be added to the polymer compositing to take advantage of the absorption of a functional polymer to the particle surface to modify the filler/polymer interface chemistry, giving rise to complete de-agglomeration of the fillers and subsequent elimination of the air void[6]. It is also necessary to adjust the solvent composition combined with the coupling agents, which is associated with coupling, adhesion and dispersion. In this study, a titanium-based coupling agent and a typical solvent mixture were selected and formulated with a paraelectic filler and a phenylene-based polymer. The optimum amount of the coupling agent was determined by the viscosity response for various levels of the application of the coupling agent. The de-agglomeration effect was pronounced when significant reduction in suspension viscosity was observed. Optimal combination was formulated to make RF capacitor laminate that used thin dielectrics having thickness range of 12–25 µm.

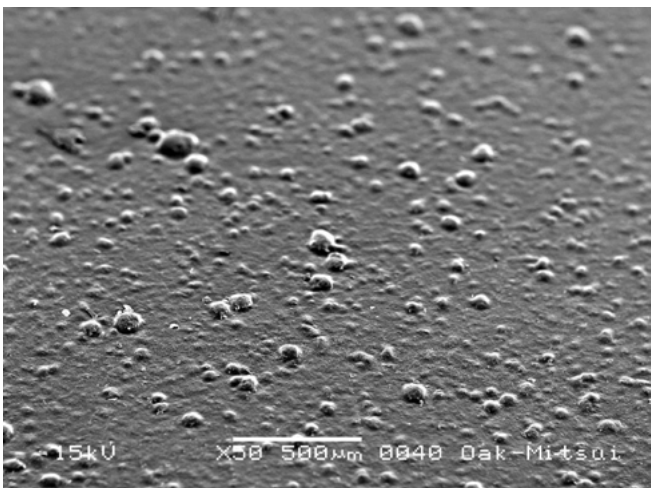

Figure 1: SEM image (at tilt angle) of the typical filler agglomerates of ceramic filled polymer composites (on the coating surface).

II. Results and Discussion

A. Effect of Ceramic Functional Particles (Fillers)

For practical device application, the contribution of the filler to the dielectric strength and the temperature stability of the capacitance are of greatest interest. The dielectric strength was examined by measuring dielectrics breakdown voltage (BDV) of the samples having fillers with different size (Figure 2). A circular pattern with 0.5 inch diameter was placed on a bottom electrode grounded to the DC tester. A probe was placed on the center of a circle and subjected to the voltage. The electrode material was made on one side of the copper of a RF capacitor lami-

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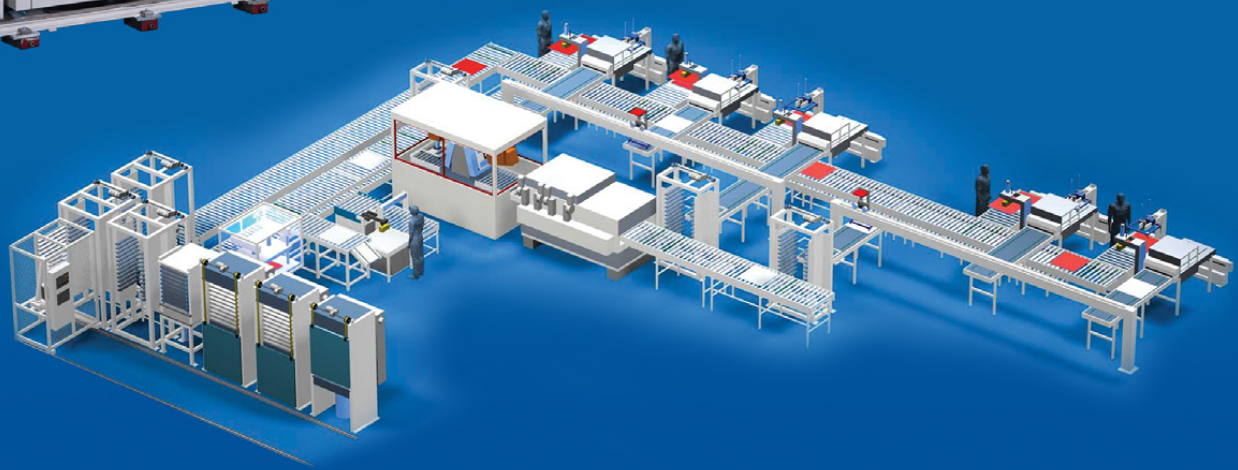

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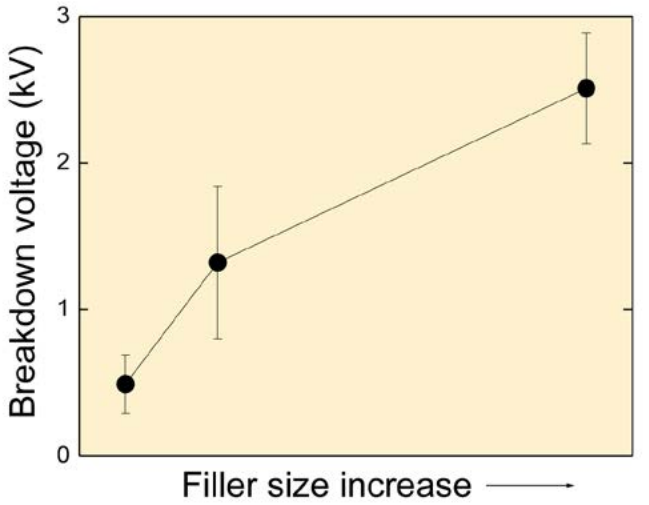

Figure 2: BDV variation of polymer compositing with the filler size.

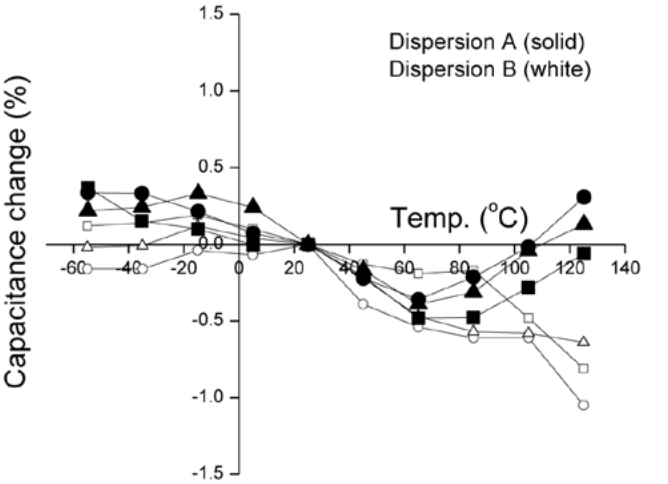

Figure 3: Temperature stability of capacitance of two samples prepared by different suspension preparation routes.

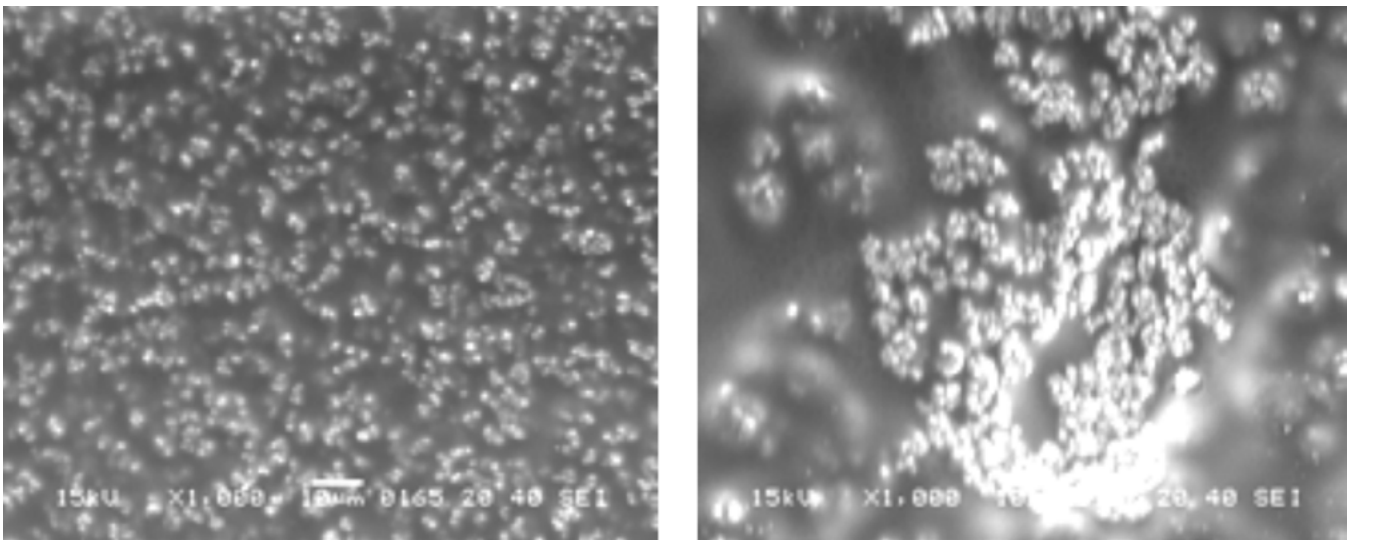

Figure 4: SEM images (on the coating surface) of samples with (a) dispersion condition A and (b) dispersion condition B.

nate. The dielectric thickness was set to 25µm for all samples. As shown in Figure 2, the effect of the filler size on the BDV was clearly detectable, and the BDV of the dielectrics composed of the larger size filler revealed a considerable improvement in BDV compared to the case of formulating with the smaller size filler. Lower BDV may result from non-uniform dispersion of the filler and it may induce the charging of the weak interface chemistry, probably representing the filler agglomerates. We continue to work on improving the material to achieve relatively high BDV even with small size filler by controlling the suspension chemistry.

Indirect evidence for the improvement of the filler distribution was sought by measuring capacitance change with temperature for samples fabricated with different suspension preparation routes. Temperature coefficient of capacitance (TCC) is an important material pa-

rameter to meet the tighter RF/microwave design tolerances. (Details on TCC were described previously[7]) Figure 3 shows that the TCC was rotating counterclockwise (direction to the positive TCC) toward the end of each curve at high temperature region. We mixed fillers with the polymer in an arbitrary way. Thus, in this physical construction of the polymer compositing, the dielectric is comprised of filler and polymer with the filler occupying the majority of the dielectric. The filler selected ended up slight positive TCC and the plain polymer (without filler) showed negative TCC. The filler contribution to the net composite TCC is dependent on its volume fraction and distribution. Therefore, it is assumed that the filler can control complete TCC by compensating for negative TCC of the polymer and positive TCC at higher temperature could be regarded as being responsible for the uniform filler distribution in the polymer matrix. SEM photos in Figure 4 supports this with different level of dispersion of the filler in polymer between two samples.

B. Characteristics of RF Capacitor Laminate

Figure 5 shows frequency stability of Dk (dielectric constant) and DF (dielectric loss) of our developed RF capacitor laminate product using the ceramic-particle-filled polymer composite. As for the method for checking Dk and DF, the first point in Figure 5 used the lower frequency method (LCR meter) and the remaining three used the split post resonator cells which is useful to measure Dk for isotropic mixtures (when fillers are randomly oriented)[8,9]. The product is the copper clad laminate (CCL) with a standard panel, 18 x 24 inches. It was composed of two sheets of copper foils on both ends with organic based composite dielectrics having fillers dispersed into polymer in between. Copper foils are available in various thicknesses, 0.5 ounce and 1 ounce being the dominant thickness, but thinner copper foil would help to minimize the variation in capacitance during etching process in PCB manufacturing. The typical Dk and DF of the RF capacitor laminate at 1GHz were measured, 7.8 and 0.0022, respectively. We are expanding the product's capacitance density range up to 670 pF/cm^2 thinning dielectrics and

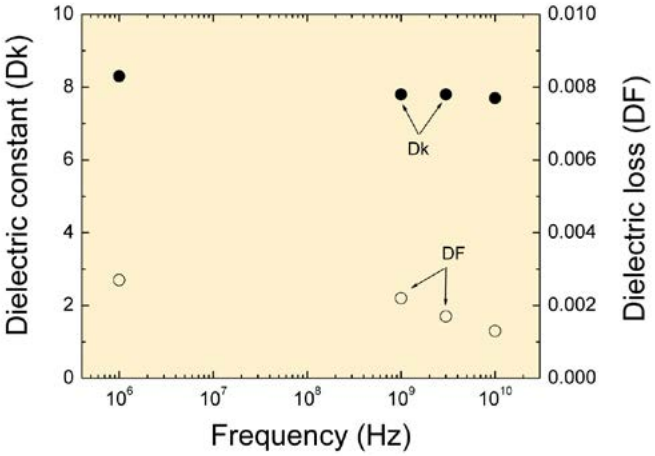

Figure 5: Frequency dependence of Dk and DF of the developed RF capacitor laminate.

process optimization. The standard reliability tests including solder shock, solder float, time to delamination and THB (temperature, humidity and bias) testing were performed and all these tests passed.

C. Uniformity of Capacitance

Capacitance tolerance for the organic-based RF capacitor laminate is critical for the application of forming discrete type embedded capacitors inside the organic packaging substrate. In this case, capacitance tolerance can be expressed as 3 sigma in the form of (mean of capacitance) ± (3 sigma) for the foot print size of the capacitor. Smaller tolerance in capacitance is desirable to achieve better yield performance of the RF device in manufacturing[2]. However, when forming discrete embedded capacitors inside the organic substrate for RF module, the materials and processes don't currently allow for the tight tolerances due to the material and the process variation. The dispersion techniques for the ceramic fillers in polymer and the right coating method for putting the ceramic-filled polymer composite material on the copper can minimize the material variation. In addition to the material variation, the process variation (mainly etching variation) in formation of the electrodes by the etching process in PCB manufacturing will add to the tolerance. In order to understand the capacitance tolerance of the

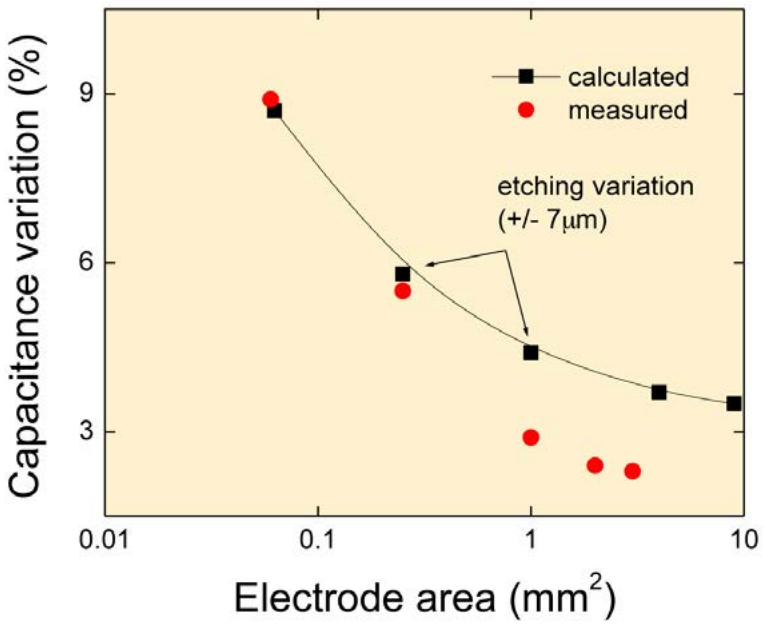

Figure 6: Capacitance variation with electrode area: calculation vs. measurement result.

capacitor laminate, uniformity of capacitance was investigated as a function of various capacitor electrode areas (0.25 mm square ~ 3 mm square) which were prepared by the standard etching on the test board. Figure 6 shows a typical result, showing the measured capacitance tolerance and calculated tolerance (expected) of capacitance. Actual measured uniformity of capacitance in smaller foot print of the capacitor showed a good correlation with an assumption that the etching variation is around ±7μm. Small footprint capacitors with tight tolerance is still being challenged, but the result in Figure 5 indicate that we can still achieve fairly uniform capacitance values with proper process optimization and control that will result in functional RF circuits.

III. Conclusion

The ceramic filled organic-based composite material has been used to make RF capacitor laminates (to compete with ceramic chip capacitors). Using this material, we successfully achieved low DF of ~0.002 at GHz frequencies (up to 10GHz), higher dielectric strength and better TCC by optimizing size of the filler and controlling its distribution in the polymer matrix. This material can be applicable for the use either in discrete RF components or in being embedded within the packaging substrate as an embedded RF capacitor material. **PCB**

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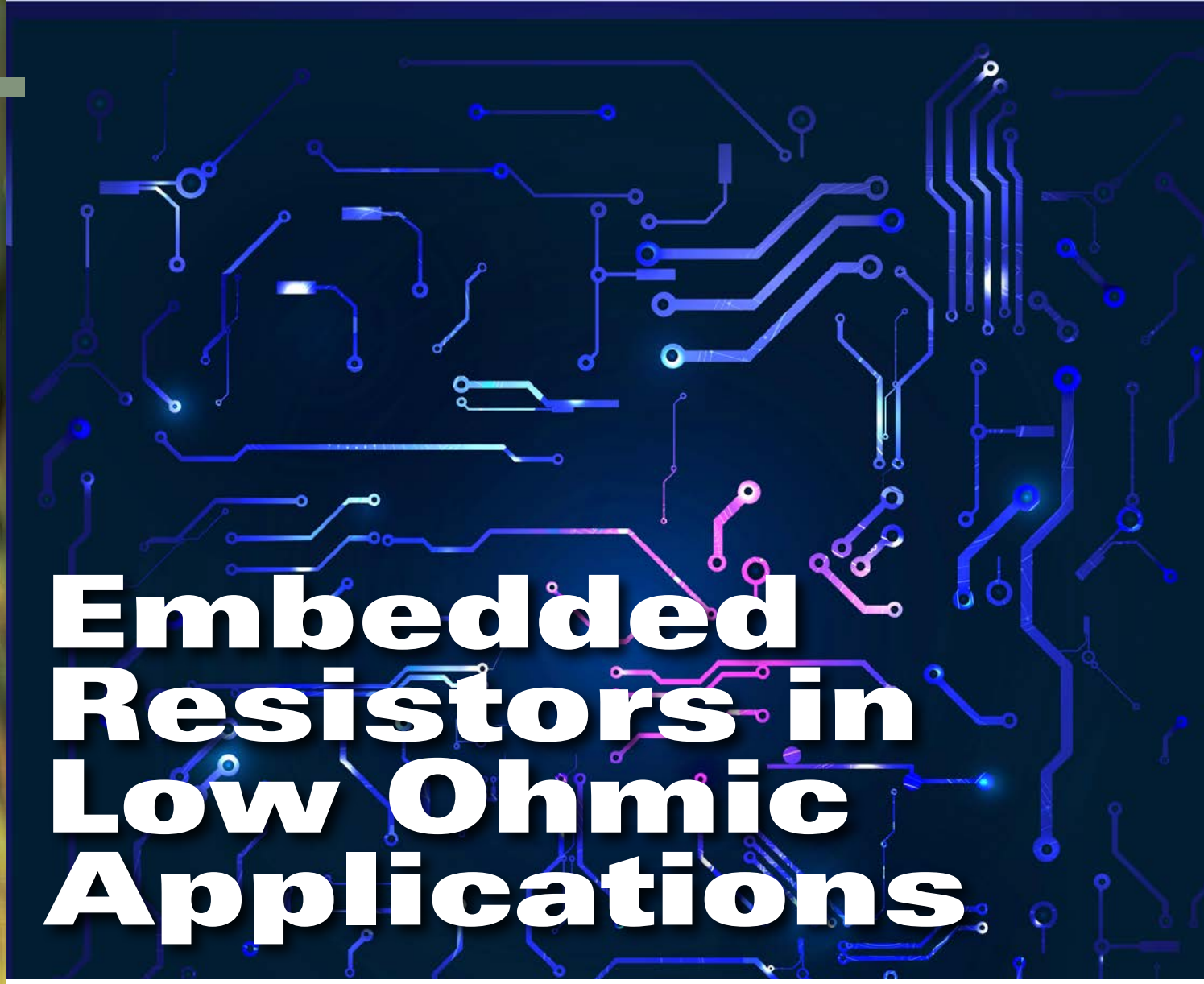

Embedded Resistors in Low Ohmic Applications

by Daniel Brandler and Manuel Herrera
OHMEGA TECHNOLOGIES INC.

Summary

Industry trends of smaller, faster, more modular "plug'n play" type devices are challenging designers to find alternative interconnection methods and related technologies. Increasing I/O densities in smaller form factor devices result in the need for embedding passives within PCBs. Embedded resistors are one such technology with a long pedigree of high reliability and proven performance.

Introduction

The reasons for using embedded resistors are simple: size, performance, and reliability. The electronics industry continues to push the envelope of how much can be packaged into smaller and smaller areas while the speed and I/O densities of integrated circuits continues to increase. The PCB designer is faced with the daunting task of trying to route circuitry in less area while still preserving space to accommodate both active and passive devices necessary for proper system operation. This has led to a growing use of HDI boards with ultra-fine lines and buried/blind via technologies. Embedded resistors are complementary to HDI technology, with removal of passive devices from the board surface enabling more real estate for active devices and allowing shorter interconnects between the I/O and the resistive element. Other benefits of embedded resistors are reduced EMI, lower inductive reactance and greater reliability with the elimination of the surface resistor assembly and solder joint.

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Sheet Resistivity (Ω/□)	Material Tolerance (%)	Typical Applications
10	3	Developed for series termination resistors as ORBIT® (Ohmega Resistors Built In Trace) and also used for other applications, like flexible heaters
25	5	Used primarily for series/parallel termination resistors and power dividers
50	5	
100	5	Used primarily as pull-up/pull-down resistors for electronic logic circuits

Table 1: Available Sheet Resistivity and Typical Applications.

Embedded resistor technology, primarily used in performance demanding military, aerospace and high density computing applications, has been increasingly used in the high-volume consumer electronics market. This migration into the consumer segment is happening because designers can use embedded resistors as a solution to tight space constraints. Embedding can free up PCB real estate, reduce via and layer counts, eliminate the need for components on the bottom side of the PCB, and eliminate common quality issues found in passive component SMT processes.

The performance benefits of embedded planar resistors can also be seen in high-frequency switching applications where the parasitic inductance of SMT components has an impact on performance. Reducing the parasitic effects improves signal quality.

For this article, we are defining low-ohm values as greater than 10 ohms and less than 100 ohms. The advantage of embedded resistors in this range of resistance is realized in high-frequency data communication and front-end RF circuits.

Embedded Resistor Applications

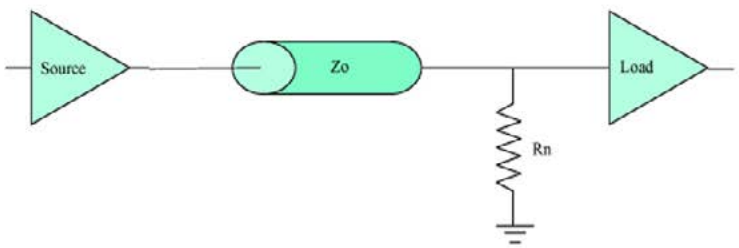
A variety of resistor values can be achieved using embedded resistor material. The table below shows available OhmegaPly® resistor values based on type of application.

Termination resistors in high-speed digital communications are a prime application of embedded low ohm value resistors.

The ohmic value of any resistor (R_n) used to terminate a high-speed digital signal is a function of the device impedance (Z_n) and/or the characteristic impedance of the circuit (Z_0) as shown:

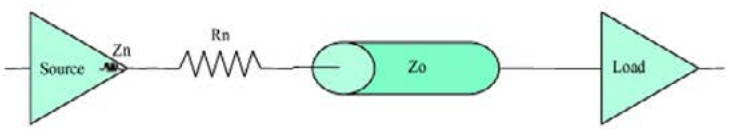
a. Parallel termination

$R_n = Z_0$



b. Series termination

$R_n = f(Z_0, Z_n)$



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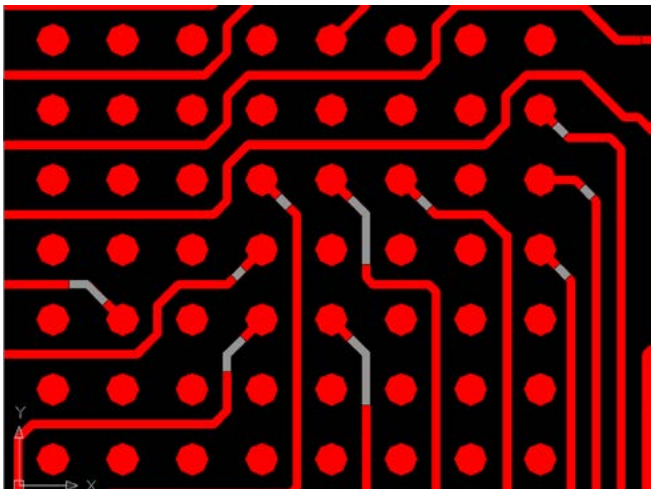

Figure 1: Example of ORBIT layout.

Terminating resistors are used to reduce signal reflection and maintain proper signal integrity. OhmegaPly embedded resistors can be placed very close to the end of the driveline, improving impedance matching and reducing line delay.

For fine-pitch BGA packages where the channel widths between the pads surrounding the interconnecting vias are insufficient for standard resistor footprint designs, resistors can be formed as part of the internal logic trace. A 10-ohm per square sheet resistivity product specifically designed for low value series termination has been used for more than 10 years in this manner.

Built-in-trace resistors simplify designs by eliminating the resistor footprints under the SMT components. The resistor width equals the trace width, but the resistor length is not limited (because the resistor can always follow the trace). Typical trace widths, and hence resistor widths, are greater than 125 µm.

With the introduction of micro-ball grid arrays (µBGAs) with pad pitches of less than 500 microns, the channel width is reduced to the point where there is insufficient space for standard built-in-trace resistor elements. Resistors with line widths less than 100 microns are required[1].

The necessity for smaller line width resistors with good tolerances and power lead to the development of an optimized OhmegaPly alloy with improved chemical and physical stability. This improved material has the ability to create built-in-trace resistors less than 50 µm wide. Embedded resistors within 0.3 mm pitch µBGA or PBGA packages are therefore achievable where line and space widths are about 40 µm[2].

Embedded Resistors in Dual In-Line Memory Modules

Higher memory speeds in DIMM modules requires termination of the bus to manage ringing and reflections. Typically these termination values will be 15–55 ohms. For example, approximately 100 resistors can be embedded on a DDR3 RDIMM module and roughly 90% of those resistors are below 40 ohms[3]. The use of embedded resistors allows designers to place resistors where traditional SMT components cannot be placed. This improves signal integrity by placing the series termination or buffer resistors closer to the source and removes the restriction of placing along the board edges. A prime example of performance improvement is seen when making a qualitative comparison of noise levels on signals when using an embedded resistor and an equivalent SMT component[3].

Embedding low-ohm resistors frees valuable board area which can result in larger memory modules by using larger DRAM chip footprints or production of a simpler board by removing the resistors from the assembly process.

Earlier this year, JEDEC released a standard for design of DDR3 204-pin unbuffered SO-DIMMS using embedded resistors[5].

Multi-Chip Modules

Multi-chip modules commonly referred to as MCMs or SiPs are devices that combine multiple integrated circuits, semiconductor dies or other discrete components on a unifying substrate. Layout routing in such small footprints need to minimize vias and interconnections between layers. Some of the challenges of designing an MCM have been solved by using embedded resistors. Embedded termination resistors built-in-traces have the benefits of improving signal integrity and eliminating the extra space for SMT resistors. Again, typical resistor values needed for impedance matching are in the range of 15–51 ohms[4]. High-speed digital and RF SiPs such

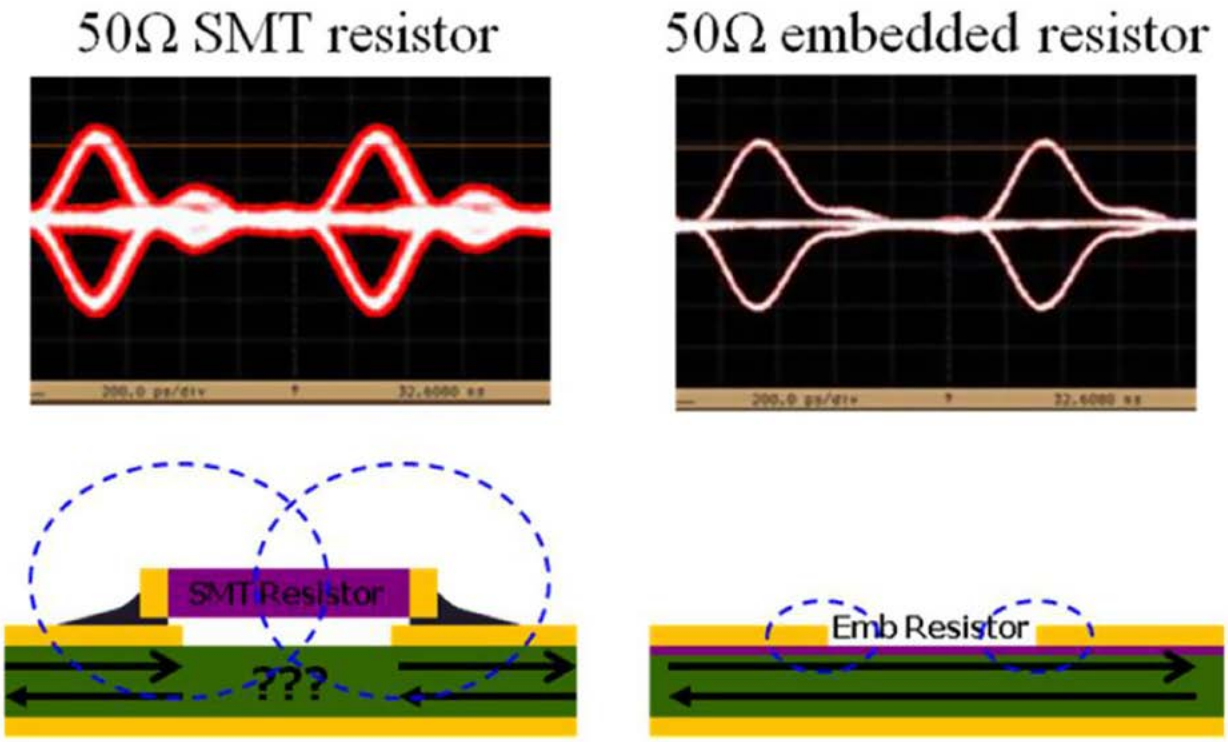

Figure 2: Signal integrity improvement with embedded resistor.

as wireless cellular and connectivity devices like Bluetooth are becoming smaller. Embedding resistors has and will continue to be an option to help designers shrink their products.

Conclusion

Industry trends of smaller and faster devices are challenging designers to find alternative interconnection methods and related technologies. Low-ohm embedded resistors built-in-trace are one such technology that should be added to any designer's arsenal of tools. **PCB**

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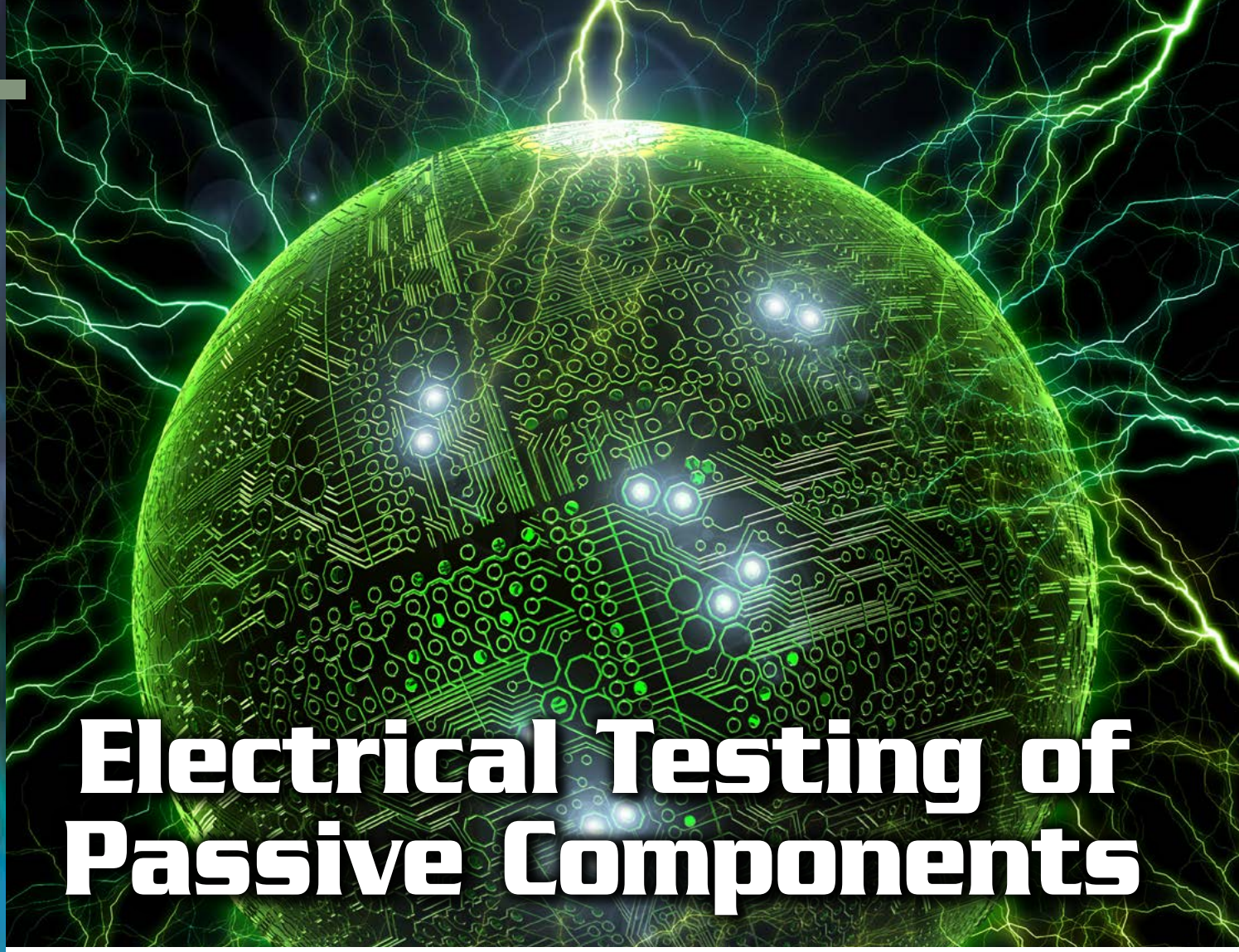

Electrical Testing of Passive Components

by Todd L. Kolmodin, Manfred Ludwig, Howard Carpenter and Rick Meraw
GARDIEN SERVICES USA AND CHINA

Introduction

Substrates have become more critical with regard to pitch and density in today's designs with challenges for passive components in terms of surface placement. This negates the opportunity for high speed, high cost components to be placed on the surfaces of the PCB. With this the capacitance and resistive components have to be embedded into the design. This has been accomplished with the advent of buried capacitance cores and buried resistors. Unfortunately, this has caused some challenges to the ET test centers/labs in the ability to effectively test these buried passive components. Processes have had to change and adapt to these new technologies. The paper will discuss what these new technologies are and how the electrical test arena has adapted to provide accurate testing of the buried resistors and accommodate the buried capacitive cores to not receive false errors from the grid testers and flying probes.

Resistors

In the past, pull-up, terminating and voltage dividing resistors have been placed on the surface of the PCB. Early applications were standard carbon resistors placed on the board utilizing plated through-holes.

As can be seen in Figure 1, the standard carbon resistor took up a lot of space on the PCB. You will also notice in the photo that capacitors are also stealing valuable space from the surface topography. As time progressed, SMT technology was introduced and the older, bulky standard carbon resistor was replaced by the newer SMT packages (Figure 2).

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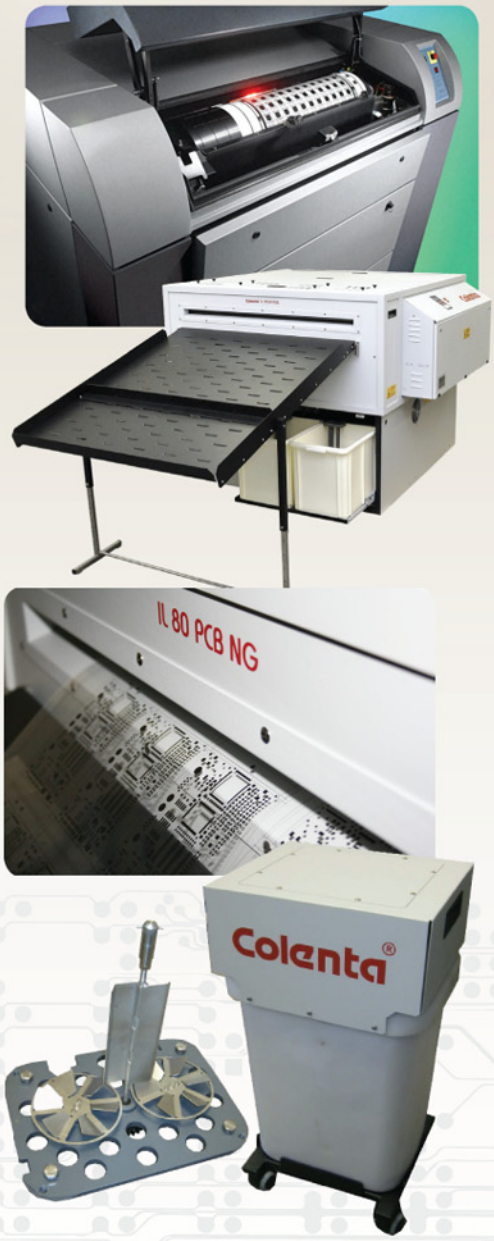

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Figure 1: Carbon resistors (as noted by their color rings).

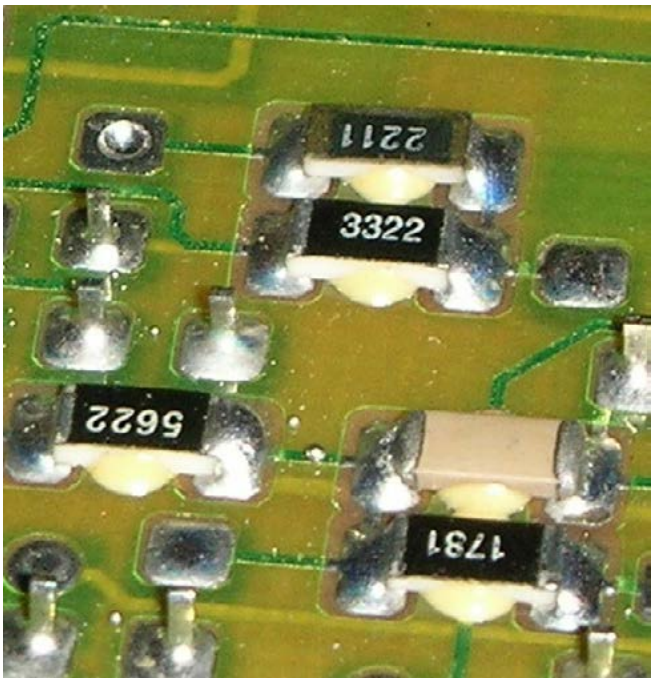

Figure 2: Surface mount resistors.

This was a very popular innovation to the industry as now the surface footprint was drastically reduced and the topography on the surface of the PCB was now open to accommodate more active components which reduced the overall size of the PCB but also allowed the complexity of the designs to grow. No longer was a PTH as needed for the resistor, which allowed the multilayer to expand its capabilities on the inner layers to provide not only an overall smaller PCB but a more powerful final product.

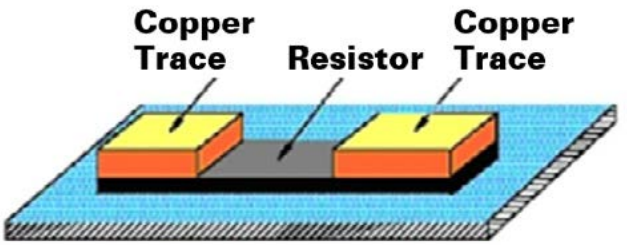

Figure 3: Thin film embedded resistor.

These technologies reduced the footprint of the PCB, but by no means could we have the smartphones, tablets and many day-to-day devices we know and rely upon today. Further it would be impossible to use the older technologies of yesteryear to power the mammoth Internet infrastructure that we take for granted today. Something still had to change. The next evolution was to hide the passive components completely from the surface of the PCB and allow the needed high power footprints of the BGAs, micro BGAs and HDI components. As of now these high speed components have challenges to be buried in the board design due to their size and the need for heat dissipation. However the passive components could be. The buried passive component allowed the ability to provide the pull-up, terminating, current limiting and voltage dividing properties without taking needed real-estate from the surfaces of the PCB.

There have been many options of the buried resistor. This spans from the carbon ink screened resistor through to thin film resistor conductor material.

This technology allows the ability to develop a buried resistor by the use of a resistive core laminated into the PCB itself. By etching away a "square" or a multiple of them, a specific resistance can be achieved. There is no longer any "hard" component.

But this now provides a unique challenge to the electrical test arena as they need to test this product with the buried signature and also certify the board to the end-user specification, be it IPC Class I, II, III or 3/A. Many times these resistors are chained in series or used in parallel, which does not allow the conventional electrical test machine to provide a "pass." Trying

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A. Explanation of Ohms-Per-Square

The resistance of a OhmegaPly® resistor:

$$R = R_s \frac{\text{Length of Resistor}}{\text{Width of Resistor}}$$

Equation 1

Where R_s is the sheet resistance (in ohms per square) of the PRT material. The resistance value of the resistor can be determined by sheet resistance and geometry of the resistor according to the formula above.

$$R = R_s \times N$$

Equation 2

Where N is the number of squares ($N = L/W$)

Figure 4: Thin film resistance calculation.

to test these buried resistors by conventional means only results in a "fail," as usually the resistance is higher than the IPC class requirement. Further, care has to be maintained to not compromise the resistor itself due to excess current applied.

When we are testing the buried resistor we must take into account the power dissipation of the given resistor. As we know, if we apply too much current to a resistor and overload its power dissipation rating, the resistor will burn.

Testing Resistors

Electrical testing is required to validate the correct resistor values and also identify faulty or out-of-tolerance resistors. It is recommended that electrical test be performed on both the innerlayer and the final board so that if a resistor is faulty at the innerlayer stage it can be scrapped prior to any further value-add to the PCB. Netlist testing must be used as a learn-and-compare type of test, which cannot validate the expected value. Most of today's CAD/CAM systems have the ability to output tester data with inclusion of the buried passives. The IPC-356A data format provides the inclusion of the buried passives. What must be included are all the resistor locations or test points, the expected value and the upper and lower tolerance values. There are a few different options for testing the resistors. This can be the use of a universal grid tester (bed-of-nails), a flying probe tester or the use of a manual measurement system. In the end, the accuracy of the readings will depend on the accuracy of the metering system being used, the amount of copper between the test probes and the actual resistor, contact resistance and the resistance of the probes and leads. Most important is that the measurement current should not exceed the current carrying capacity of the resistor. This could lead to permanent damage of the resistor.

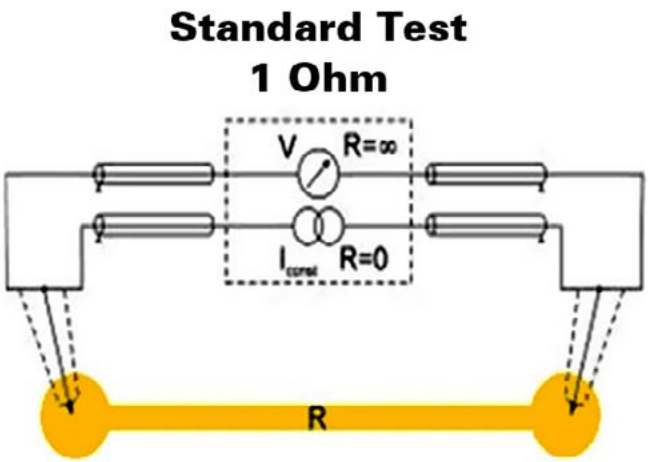

Figure 5: Resistor measurement with current limiting.

For most automated test systems the following guidelines should be applied:

1. Input the power rating (watts) of the resistor, if this feature is supported by the test system
2. Limit the test current used to 20mA

A flying probe (or grid test) machine basically contains a high-speed ohmmeter that allows rapid gathering of resistance values for nets on the PCB.

Once the resistor value is known the machine will make the necessary tests to the resistors and catalogue the results. It will compare the expected value with the read value (compensating for the allowed tolerances) and internally log the resistor net as pass or fail. Once the entire test of the PCB is complete, a report ticket will be printed, stating that the PCB has passed or failed and identifying all resistors that failed in addition to the standard continuity test results. Many machines of today can also supply a report of all the resistor values read for the given PCB for statistical process monitoring.

Protecting the Resistors

When testing the resistors via a flying probe, care must be taken to limit the voltage/current drive to the measurement. Flying probes have two methodologies when taking measurements: constant current and constant voltage. Depending on the design of the flying probe you have could cause some concerns. If the BR record was provided in the raw netlist the machine should make the appropriate determinations of how to best test the resistor. If the system is solely constant current source (grid/prober) it should be able to automatically detect if the test parameters are in range. If the system has constant voltage capability, then it can auto-range itself to the appropriate power level. A constant current system is only limited by its internal supply voltage. With a constant current scenario the actual power or "wattage" is not monitored and can be detrimental to the UUT. The constant current method is far too restrictive for the range of resistors that are in use today. These measurements should be done in a constant voltage mode. In this scenario the current is based on the actual resistance read and not the calculated or anticipated value. In this scenario it is a simple calculation of E*I, where E is the voltage applied and I is the current. In a constant voltage scenario the resistance is only needed to calculate the required voltage of the source. The measurement parameters are constructed using the E=P/I formula where E =Voltage, P=Power and I = Current. The measurement is taken at the calculated E and the resultant I is measured and calculated in ohms.

Capacitors

Just as with the buried resistors, capacitance can also be embedded into the PCB. This is done by the use of a capacitive core material laminated into the PCB. This removes the need for surface decoupling capacitors and as with the removal of some of the surface resistors allows more space on the surface of the PCB and allows the overall size to be reduced.

However this introduces a challenge with electrical test. With the buried capacitance in the PCB false shorts can be reported by the tester. The standard electrical test for shorts applies a voltage (primary point) and reads for current leakage on adjacent nets in the case of the flying probe or any nets in the case of the bed-of-nails grid test machine. A specific threshold is set on the machine so that nets to one another

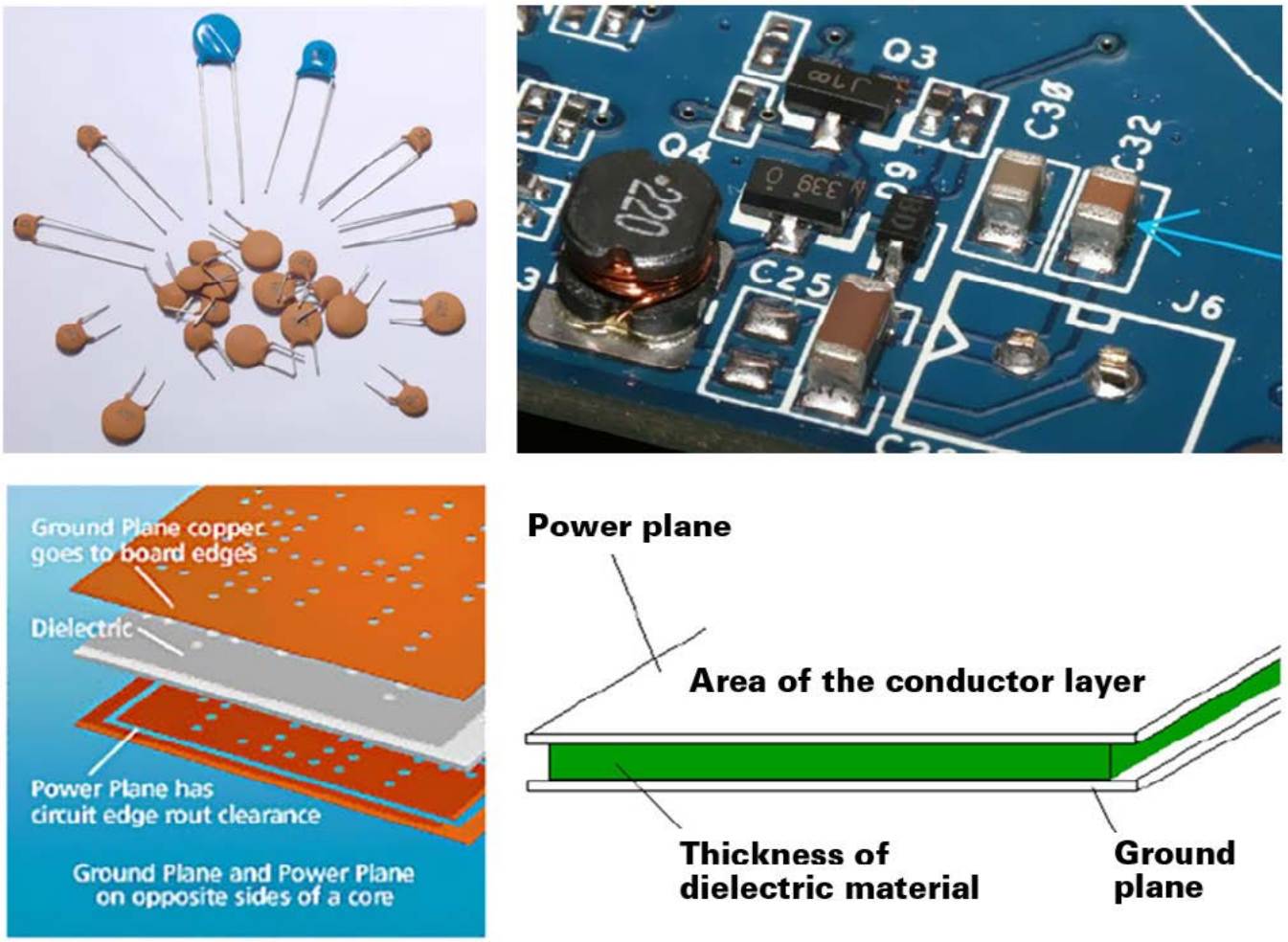

Figure 6: Various capacitor evolution, clockwise from upper left: ceramic paper, SMT and buried capacitive cores.

must have a minimum resistance between them or a failure is reported. For example, IPC-9252A Class III specifies greater than or equal to 10M ohms. This measurement is taken very quickly and due to the capacitive charge time the test machine may report this momentary leak as a false short.

Testing

Grid Test

Unfortunately one finds that many of the older grid test machines have no solution for negating this capacitive charge component. Newer machines have the ability to delay the measurement for a specified time to allow for the capacitive charge to stabilize before the reading is taken. This is relatively transparent to the operator. Once the test is initiated the continuity test is performed as normal. When the isolation (shorts) test begins the machine applies the test voltage to the PCB and then waits during the input delay time before taking measurements. This allows the capacitive core to charge and stabilize. The end result is a pass rather than a false error reported.

Flying Probe

These machines have the same dilemma when testing PCBs with buried capacitance. Flying probes do not by default test every net to every net for shorts as the grid test machines

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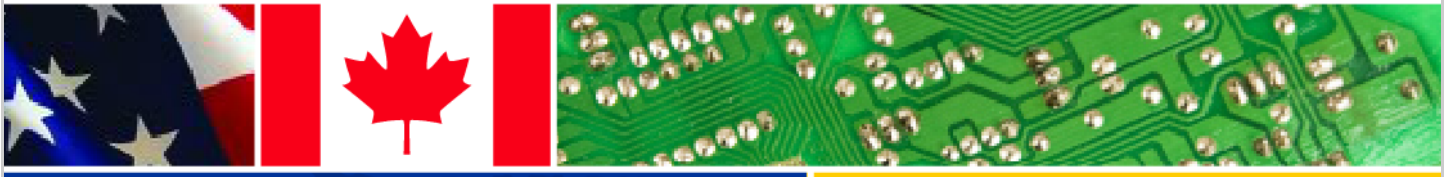

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do. Flying probes use what is called adjacency testing for shorts. One reference probe is set on a net and the other probes measure for leakage in adjacent nets. This window is defined during the CAM process. As with the grid test machines the same charge time variable is introduced and can cause false errors to be reported. Earlier software packages driving these machines did not have an accurate way to delay the reading and they were not able to provide a pass to the product which required a manual verification of the error and a human decision made to whether the board was good or not. This was the same with the older grid test machines.

Some newer software packages for the flying probers did in fact incorporate delay timers to combat the capacitive charge. However these timers were applied to the entire test which would slow the machine down. Although it was a solution it adds time to the overall test on the flying probe. Another known software package for the flying probe introduced a bit of AI to the test routine which actually monitors for this charging variable. This allows the machine to run at full speed until it detects a possible short. It then falls into a delay routine and takes multiple measurements of the suspect net to determine if it is a capacitive charging variable or an actual short. If the resistance between the two nets charges and a stable resistance reading is obtained within the test parameter threshold the machine will pass the network and move on. If the leakage continues in excess of the timer measurement threshold a true short is indicated and the net will be flagged as a failure. This advantage allows the overall test time of the PCB to remain optimal rather than slowing down every measurement reading resulting in lost velocity and throughput.

If the resistance between the two nets charges and a stable resistance reading is obtained within the test parameter threshold the machine will pass the network and move on.

Conclusions

As technology grows and PCB sizes shrink the demand for embedded technologies will only grow. Many end-users are designing embedded passives into their products and the electrical test community is expected to provide the test solutions for these new powerful designs. The use of buried resistors is increasing and care must be taken to identify these components during the ET CAM process so that the test machines are aware of them and do not overpower them with standard test parameters. For the design community that uses the buried core technology the manufacturers of this material have always recommended using the largest configuration for the buried resistor as feasible. As noted previously the square should be as large as feasible to provide the required resistance while also maintaining the optimum power dissipation level to ensure long life and stability.

Buried capacitance has been around for a long time but is also increasing. The ability for electrical test to accurately test this type of product is crucial. Accurately identifying and allowing the buried capacitance component results in improved throughput and delivery. It also reduces unnecessary delays, troubleshooting and unfortunate scrap of product that is actually good. **PCB**

Todd Kolmodin is the vice president of quality for Gardien Services USA. To contact Kolmodin, click here.

Manfred Ludwig is director of operations at Gardien Services China.

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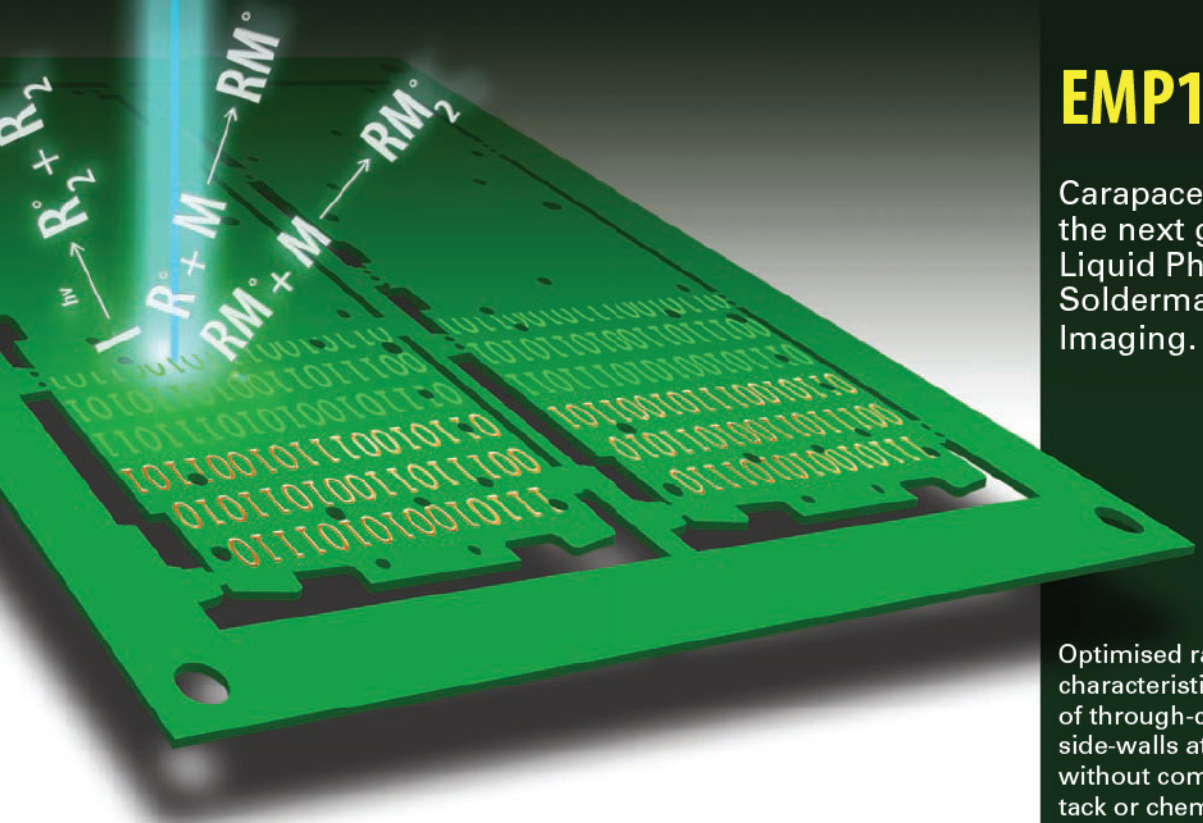

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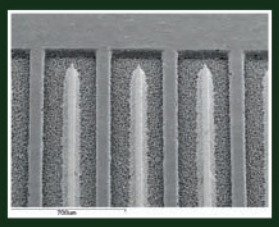

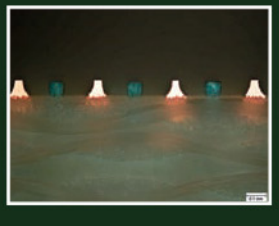

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READER RESPONSE

Gerber—the Smartest Way Forward

Editor's Note: *This response refers to an article by Mentor Graphics' Julian Coates, which ran in the February issue of The PCB Magazine, and was received in early June. Mr. Coates was given the courtesy of a rebuttal so they could be published side-by-side in the same issue. The rebuttal follows.*

In a recent an article by Julian Coates of Mentor Graphics, Smart Data Formats Automate CAD/CAM (*The PCB Magazine,* February 2014), in which Coates promotes more widespread adoption of the ODB++ format, the arguments he uses indeed make it seem like OBD++ is the great panacea for our industry, one that promises to eliminate all problems for CAD-to-CAM data transfer without any downsides.

In order to promote ODB++, Coates unfortunately reverts to Gerber-bashing rather than explaining the strengths of ODB++. And his arguments are highly misleading, as they are based on some tired old fallacies that I would like to address here. Before starting, though, it's important to clarify that when referring to Gerber, I mean RS-274X Extended Gerber, the current Gerber format. This supersedes the earlier RS-274-D Standard Gerber format, which is obsolete. Bashing RS-274-D Standard Gerber is like railing against Windows because MS-DOS only allowed eight-character file names. If Coates wants to bash RS-274-D, I'll gladly join him. Having said this, less than 2% of all jobs are transferred using the old format, so it's practically a non-issue.

Extended Gerber is the PCB industry's de facto image data transmission format. New formats have come and gone; some, like the ODB++ format, have been around for decades, but still today, more than 90% of the world's PCBs, from the simplest to the most complex, are still manufactured using Gerber, which tells me that this is an image format that the industry trusts. And the industry is right to trust it—it's the best there is. Used properly, it delivers on its promises, without fail, every time.

So let's have a look at some of Coates' arguments. He quotes Viasystems as stating that, "about 25% of the data packages they receive have issues relating to:

- Missing layers, fabrication drawings, drill files, etc…
- Netlist format violations
- Netlist exception violations."

If true, this is indeed a sorry state of affairs, and needs rectifying. But if this is the extent of the problems, then there is nothing wrong with the format. Viasystems' issues are in fact due to some rather trivial bugs in the CAD vendors' implementations, so the solution is to fix the implementations rather than to adopt completely new software by switching to a new format. The article is not clear about whether these omissions and violations relate to ODB++ or Gerber files, or a mix of the two. However they arise, I can only recommend that Viasystems report these issues to their customers with a request to contact their CAD software suppliers. If the CAD software vendors fix these simple bugs, the issues will be resolved once and for all. If they are unable or unwilling to do so, there is no solution: neither in Gerber, nor in ODB++, nor anywhere else for that matter.

Coates also mentions that Gerber files sometimes contain syntax errors, low numerical accuracy and other errors. This is no doubt true, but again these are simply bugs in the Gerber output. Do we need a new format to fix syntax errors in the current one? Surely the solution is to fix the bugs in the Gerber output. And ODB++ itself is not immune to syntax errors; if anyone would like some invalid ODB++ files, I can provide a few.

The reality is that Gerber files very rarely generate the wrong image. This is because while

only a few applications read ODB++ reliably, there are countless more that read Gerber with near-perfect reliability. This is because:

- The Gerber format is simple
- Its specification is well-written, easy to read, detailed and precise
- Most of its implementations are mature
- As it is so widely used, the implementations are thoroughly field tested, so most bugs have been ironed out
- The format is supported by excellent free viewers such as GC-Prevue

Advocating the adoption of a new and much more complex format to eliminate simple bugs is a very curious solution indeed. Consider only that a CAD software developer struggling to produce a simple Gerber file correctly is not miraculously going to write a bug-free implementation for the more challenging ODB++ format. If one wants bug-free software it is best to stick with Gerber, as Gerber is a simpler and more mature format than ODB++, it is far less prone to bugs, and its bugs are far easier to find and resolve. Switching to a new imaging format introduces a whole raft of new issues and bugs that would take many years to sort out. Imaging software is complex and takes a long time to get right. Adopting ODB++ to solve bugs in Gerber output is like using a sledgehammer to swat a fly: The solution is far more damaging than the issue ever will be.

Table 1 summarizes Coates' claims regarding the benefits of ODB++ vs. Gerber:

Here is my take on the aforementioned benefits:

1. False. A simpler, more reliable format in fact needs less diagnostics
2. False. An error can be more easily identified in a simpler format.
3. False. ODB++ is not miraculously error-free.
4. False. IPC-356 supports the actual customer net name. It may be that the software Coates uses does not display it, but this then is a problem in that software.
5. False. Gerber has negative apertures and so can handle planes perfectly. (I should add that this is the first time I see the claim that ODB++ is more compact than Gerber!)

If these are the benefits of ODB++ and the reasons for adopting it, then Coates' argument collapses.

More importantly, Coates omits to mention the difficulties in adopting ODB++. Over the 20 years that ODB++ has been available, it has taken just 10% of the market share, with Gerber accounting for the remaining 90%. If ODB++ offers all the advantages espoused by Coates in his article, there can only be one of two reasons for its minimal uptake:

- The PCB industry consists largely of morons
- There are downsides to using ODB++

As I do not think this great industry is in the hands of morons, I believe that there must

ODB++ Benefits for the PCB Fabricator
1. Import and export diagnostics are significantly reduced compared to Gerber
2. Errors can be identified and communicated to the customer much earlier in the process
3. Eliminates format errors and net exceptions that are common with Gerber
4. Fabricator can be allowed to see actual net name used by customer, easing the process
5. Less data is required for handling positive planes

Table 1.

be some serious downsides to the adoption of ODB++. This is not because ODB++ is a particularly bad format: It is not. The point is that the adoption of ODB++ includes the adoption of a new image format, and image formats are notoriously hard to implement. Much has been written about just how complicated geometric software is and how much effort it takes to get it right, not to mention the years it takes to debug. So the implication that taking on this new image format is simple and low risk is at the very least misleading. Precisely because our industry's practitioners are not morons, they know this, so are reluctant to adopt a new format. They know very well how complex ODB++ is, and that it will give rise to many more problems, for many years.

The reality is that Gerber works very well for transferring images. In fact, there's nothing better.

Gerber X2

The most interesting point made by Coates is that Gerber files contain "no information about how the PCB layers stack up." This was a valid objection in the past, but it is no longer true, as the latest revision, Gerber X2, now contains layer stackup information.

At the heart of X2 is the use of attributes. These are akin to labels which provide information that are associated with image files, or features within them. The beauty of using attributes is that they are already familiar to CAM professionals and software developers, and they sit naturally with the current capabilities of CAD and CAM systems. X2 extends the current Gerber specifiation with a series of standard attributes that are most important for efficient CAD-to-CAM communications, such as the function of each layer, whether a pad is a via or an SMD pad, and which are the component drill holes. As rather grandly stated elsewhere, X2 adds intelligence to the Gerber format. Software supporting X2 will read the whole Gerber archive automatically, with all layers in place, while identifying the function of each object.

Easy to adopt and to implement, X2 is upwardly compatible with the previous Gerber version. Altium, global leader in Smart System Design Automation, has been quick to recognise the value of X2 and will support it in an upcoming version of Altium Designer. By Q4 2014, Graphicode's widely-used and highly-respected GC-Prevue viewer will also support X2.

X2 maintains the trademark simplicity for which Gerber has always been known and used, and gives designers and engineers a standardized procedure that will require very little to change in their working practices—certainly none that would require approval, testing and all the rest. Equally important, this new revision does not disrupt existing workflows. If the software does not support the new capabilities, the old workflow continues to operate. Nobody is forced to buy anything. So this will be a very gentle, low cost improvement indeed, but the effects will be nothing short of revolutionary.

Coates omitted to mention this latest development in the Gerber format, one of the most important developments in CAD-to-CAM automation today, given that it concerns the industry's de-facto standard format. Neither did he mention the alternative IPC-2581. Had he done so, his arguments for ODB++ might have been less compelling of course, but these omissions in an article titled Smart Data Formats Automate CAD/CAM lead to serious doubts about its objectivity.

Coates also added a diagram to the article comparing Gerber to ODB++ input in CAM. This compared a badly implemented Gerber with a well implemented ODB++. I have taken the liberty of adding a proper X2 Gerber to the schematic. The result, given in Figure 1, shows that if ODB++ is a smart format, Gerber X2 is a very smart one.

Conclusion

When CAD-to-CAM data sets use properly implemented Gerber archives, plus correct IPC-356-A files, problems in data transfer are rare. Where a problem or bug appears, the easiest, fastest and most economical solution is to fix it. This is because issues are not down to the format itself, but more likely due to its implementation in CAD software, and they are simple to resolve. The very worst solution would be to replace Gerber with the far more complex ODB++ format, because implementing a new format is never simple, quick, and/or risk free,

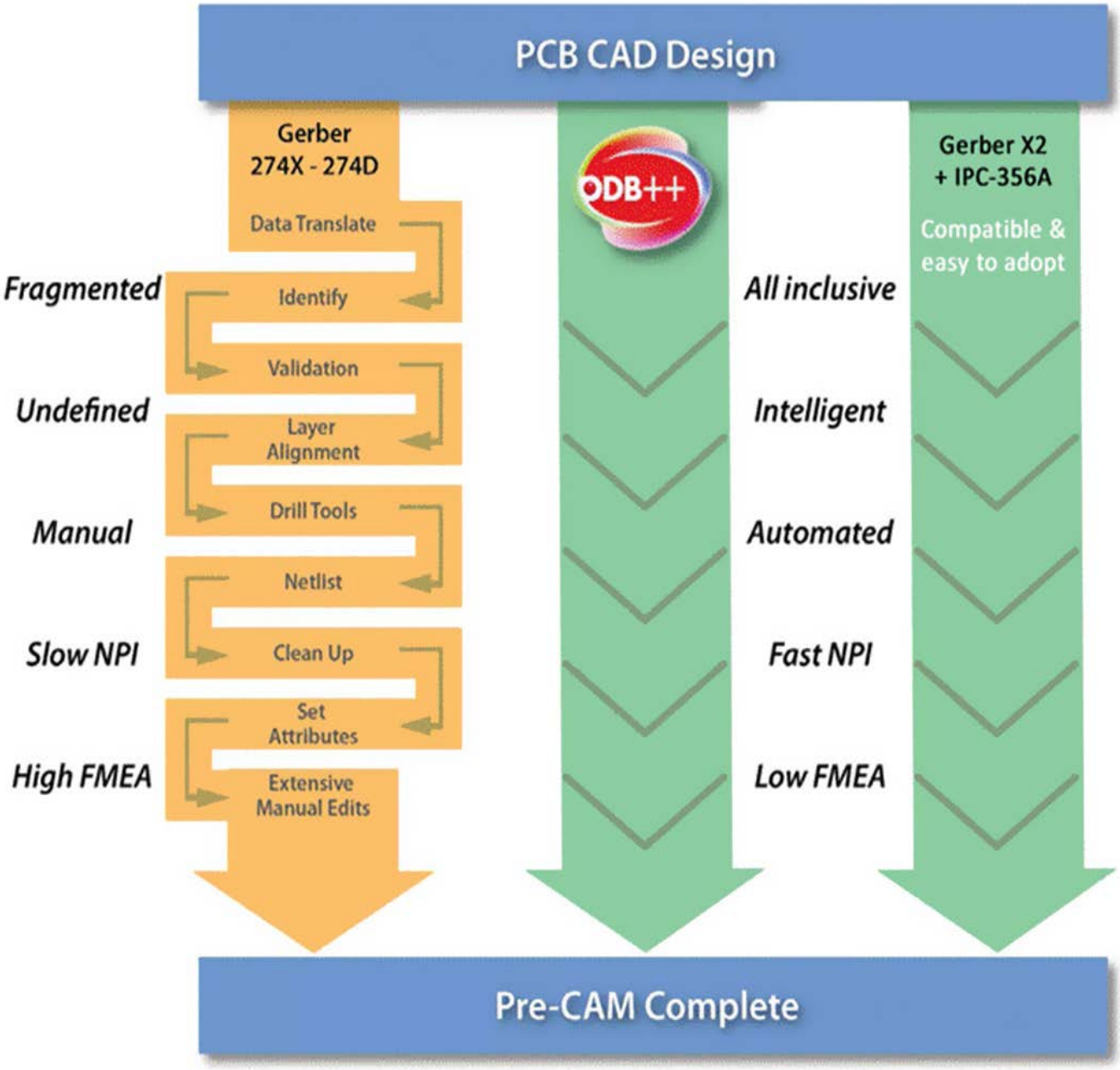

Figure 1: The column on the right can be achieved at low cost, without breaking workflows, in an upwardly compatible way.

especially when the new format is as complex as ODB++. The problems that would arise from such a move would be significant, and would hound the industry for many years.

The simplest, most practical path forward is to fix bugs in current implementations, and adopt Gerber X2 functionality.

One of the best things about this path is that it is incredibly kind on the industry, while enabling the PCB industry to benefit from all the advantages that ODB++ claims to deliver in Coates' article, but with none of the downsides. This is because it does not involve the wholesale adoption of a new format. Furthermore, the

revised Gerber format is compatible with the previous versions of Gerber and older software, so improvements can be as gradual as users want them to be, with no one being forced to buy new software against their business wishes or budgetary constraints. It is a path that delivers to small software vendors and the industry at large, fixing what is broken without compromising what already works. In short, it's nothing short of revolutionary, but without the complications.

The Gerber format specification, a sample X2 archive and background articles on X2 can be found at www.ucamco.com/downloads.

Karel Tavernier
Managing Director, Ucamco

Julian Coates' Rebuttal:

With respect to Karel, I think he may be missing the main point. Consider this:

- No doubt Gerber is a very fine format for defining the graphical layers of a PCB
- IPC-D-356 is perfectly fine for defining a netlist
- Excellon needs no improvement; it defines the location and diameter of drilled holes quite well.
- Component placement lists can define component positions and rotations quite well also
- PDF is a good format for rendering drawings
- GenCAD and FATF are good for defining the parts of a PCB assembly for testing purposes
- Word is good for capturing text, especially "Readme" documents that explain to a CAM engineer how all of the above file-types should relate to each other, and how to reintegrate all that data back together so as to enable an efficient software-driven new product introduction (NPI) process.

Certainly, if all you want is accurate graphical data, then I am sure Gerber meets the requirement, and Karel is to be congratulated on his perseverence in improving that particular 50-year-old NC format. At a recent industry debate on this topic, he suggested that the best way forward is to use Gerber for the graphical data and another format for all the other information that Gerber cannot carry. Thus, he promotes the idea of intelligent, all-encompassing formats for carrying data, but excluding the graphical part. Why reject the advantage of having all of that other information linked to the graphical objects as well, and vice-versa? The problem that needs solving is taking all of that fragemented data into a single coherent model comprising both the PCB bareboard and the assembled PCB. Keeping parts of the product-model seperate for simplicity is fine if you are only interested in a narrow subset of the PCB product-model, but it is a big problem if you need a complete definition of the product, as do all DFM and NPI engineers! There is no escape from the fact that, sooner rather than later, the data must be integrated.

Reductio ad absurdum: To take the idea to an extreme, maybe there is a drilling expert out there ready to explain that Excellon should be used for holes information, but all of the "other information" (including the layer graphics, no doubt) should be carried in ODB++. Obviously it is absurd to keep part of the PCB product-model (in this case, the holes) separate from all the rest. The first thing a CAM engineer would do in this case would be to read the Excellon file and integrate the hole data into the ODB++—an unecessarily time-wasting and potentially error-prone process.

There is a broad consensus across the industry that fixing the highly fragmented nature of the CAD-to-CAM data files problem is long overdue, and that the answer is to implement integrated,

intelligent formats such as ODB++. Many have already taken the step with ODB++, attesting to the benefits of having a more streamlined design-to-manufacturing hand-off process. Over a million different PCB designs have been processed into manufacturing using the ODB++ format since its introduction. It works, and is widely implemented by some of the largest electronics OEMs in the world, as a standard part of their NPI business process.

What limits the implementation of ODB++ more widely? Why do people still use all those fragmented narrow-scope data formats such as Gerber, Excellon, netlist, component-placement list, etc? I would suggest that the reason is not technological; it is a combination of business and human factors. Firstly, it costs money to change a business process; tools have to be upgraded. But in order to gain the time/cost/quality advantages, an investment has to be made, and that is nothing out of the ordinary. Secondly, there is a perception that continuing to use the old method is not only free but also "safe," whereas to use the new method is expensive and "uncertain." The "safe" versus "uncertain" part is the human part. There is an jargon-acronym for it: FUD, which stands for Fear, Uncertainty and Doubt. The same was true when the Gerber format was introduced. Using it required a high level of investment, and it took time for the industry to see that the benefits outweighed the uncertainties even though the idea of it was obviously a good one 50 years ago. Hand-drawn artwork was still used for many years after, even though a better method (Gerber data) was available. It took time for the industry to make the change. But change is inevitable if businesses intend to advance given the complexities of today's systems designs. This is why I advocate ODB++ as the new data format standard.

Julian Coates
Director of Business Development
Valor Division of Mentor Graphics Corporation

VIDEO INTERVIEW

IPC-7092: Embedded Standard Update

by Real Time with...IPC APEX EXPO 2014

Industry icon (and allegedly retired) Vern Solberg, from Solberg Technical Consulting, discusses recent updates to embedded components standards with Guest Editor Dick Crowe on the show floor at IPC APEX EXPO 2014 in Las Vegas.

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PCB007 Market News Highlights

The Conference Board Sees Strong, Steady Job Growth

The underlying hiring trend, especially in professional services, is encouraging, with more good news expected through the summer and into the autumn months. More jobs means more pay checks, lifting sentiment and resulting in still more consumer buying.

Industrial Robotics Market to See Steady 6.4% CAGR

In the U.S. alone, the sale of industrial robotics for manufacturing use grew by 44% during 2011, indicating that the industrial robotics market is a correlant to the overall revitalization of the production base in the U.S. and an important component of the general economic performance of the country.

Energy Capacity of Energy Storage Applications: CAGR of 71%

According to a recent report from Navigant Research, the annual energy capacity of advanced batteries for utility-scale energy storage applications will grow from 412 megawatt hours (MWh) in 2014 to more than 51,200 MWh in 2023, at a compound annual growth rate of 71%.

Automotive Electronics Market at $77B by 2020

The automotive under-the-hood ECU electronics market is estimated to have been worth US $44.8 billion in 2013 and is forecast to grow to US $77 billion in 2020, a CAGR of 8%. Semicast forecasts global light vehicle production volumes to grow over this period from 82 million to 106 million. However, more than 40% of the increase in global light vehicle production is forecast for China alone.

Printing Technologies Extend to PE Components

Printed electronics uses graphic arts techniques to print electronic and photonic devices such as screen printing or inkjet; by using conducting or dielectric inks, which results in the development of active or passive devices such as; resistors or thin film transistors (TFT).

IoT Market to Reach $1,423 Billion by 2020

The value of Internet of Things (IoT) market was worth $1029.5 Billion in 2013, and is expected to reach $1,423.09 billion by 2020, at an estimated CAGR of 4.08% from 2014–2020.

3D Printing: The Making of a $7B Market

The market has huge potential, but is still embryonic in terms of development, with main players taking their first steps by 3D printing conductive and insulating materials into a single object. 3D printed electronics, including 3D printed transistors, will not be fully realised within 10 years, but some emerging medical applications will be commercialised well before 2025.

Graphene Markets to Top $390 Million in 2024

New research by IDTechEx in the report "Graphene Markets, Technologies and Opportunities 2014–2024" shows that graphene markets will grow from around $20 million in 2014 to more than $390 million in 2024, at the material level.

Positive Outlook Develops for Global Economy

Paul A. Laudicina, founder of the FDI Confidence Index, notes, "Despite racking volatility and economic uncertainty on a global scale, the findings from the 2014 FDICI suggest that a corner is being turned. Corporations sitting on massive cash reserves are increasingly confident they can parlay these into productive investments with attractive returns."

EMS Market Driven by Demand for Testing Services

The testing services provided by EMS providers are dependent on the solutions required by OEMs and the vertical to which they cater. The outsourcing of testing services to EMS providers will increase due to innovation in consumer electronics products. The market is driven by strong demand for such services from the telecommunication and consumer electronics industries.

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IMPACT 2014: IPC on Capitol Hill "Leadership in Promoting a Strong Manufacturing Economy"

by John Vaughan
CIRCUIT SOLUTIONS LLC

Note: The views expressed in the following recap of the IPC IMPACT 2014 event held on June 10–11 are solely my own. In keeping with IPC's long-standing commitment to open dialogue by and between its members, no direct quotes or personal views from any IPC members are referenced in this article.

Although I am a Washington, D.C. native and reside in the D.C. suburbs, I must admit it was difficult not to get excited in advance about spending two days in downtown Washington on Capitol Hill at IMPACT 2014, talking circuit boards with both politicians and my industry peers alike!

As an industry, we face many challenges and obstacles in our pathway to success and IPC's IMPACT 2014 offered the opportunity to meet key members of Congress, policymakers and influencers, educate them about needed actions to strengthen the electronics sector and the overall economy and national security, and network with industry colleagues.

IPC delivered superbly on all accounts.

I last attended IPC Capitol Hill Day in 2011, and while that was an outstanding event as well, it was clear this time around that IPC had redoubled its commitment to public policy engagement. In January of this year, IPC's Government Relations and Environmental Policy office

Figure 1: IPC executives meet with President Obama's senior advisor on manufacturing policy and offer support for the NNMI.

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Figure 2: IPC executive luncheon with Rep. Bill Johnson (R-OH), an IPC champion!

moved from its former Arlington, Va. location into the heart of DC. This prestigious Pennsylvania Avenue location is just blocks away from both the White House and Capitol Hill. No big surprise, as a government outreach and member advocacy presence here clearly pays dividends. This was reflected in the steady stream of high-level meetings with senators, representatives, and White House staffers that the IPC Government Relations team arranged for our IPC member delegation.

The lawmakers our group met with included: Neil Bradley, Deputy Chief of Staff for House Majority Leader Eric Cantor (R-VA); Senator Tom Udall (D-NM); Senator Rob Portman (R-OH); Rep. Lamar Smith (R-TX); Senator John Cornyn (R-TX); Senator Mark Warner (D-VA) and Rep. Bill Johnson (R-OH).

The key messaging delivered by our IPC member company executives' contingent was structured around three interconnecting themes: supporting national security through cutting-edge defense electronics; advocating for smart regulatory reforms; and promoting technological innovation and manufacturing. These key themes were expressed in detail as follows:

Advancing Technological Innovation and Manufacturing

• Manufacturing in the U.S. has contracted significantly in the last 20 years, while manufacturing has grown in other parts of the world. IPC's member companies in the U.S. seek a level global playing field

• The U.S. government must support domestic innovation and manufacturing, including authorization and funding for the National Network for Manufacturing Innovation (NNMI)

• IPC supports comprehensive tax reform, including permanent extension of the R&D tax credit and lower tax rates for businesses

• IPC supports comprehensive immigration reform that increases the number of H-1B and L-1 visas, as part of developing and maintaining a skilled 21st century workforce for innovation and economic growth in the U.S.

Advocating for Smart Regulation

• IPC supports legislative and federal agency efforts, including the House-passed Regulatory Accountability Act (H.R. 2122) to reform the regulatory process to prevent government over-regulation that harms U.S. electronics companies in the global marketplace.

• IPC backs science-based environmental regulations, including:

– Toxic Substances Control Act (TSCA) reform that preempts a patchwork of state laws, exempts byproducts sent for recycling from unnecessarily burdensome reporting requirements, and regulates chemicals in articles only when necessary

– A Definition of Solid Waste (DSW) rule that facilitates and encourages the recycling of valuable materials consistent with the intent of the Resource Conservation and Recovery Act (RCRA).

• IPC supports SEC guidance and regulations that will lessen the burden of conflict minerals regulations without undermining the underlying goals of Section 1502 of the Dodd-Frank Act. IPC encourages the SEC to utilize the notice and comment process to implement changes in the SEC conflict minerals rule necessitated by the recent court decision that found portions of the rule unconstitutional.

Safeguarding National Security
Export Controls

• Printed boards must be subject to the same ITAR controls as the military electronics for which they are designed

• The release of ITAR printed boards to foreign individuals undermines national security; printed boards reveal highly sensitive information about the workings of the military electronics for which they are designed

• IPC supports export control reform and the publication of a final Category XI rule that clearly enumerates printed boards without relying on the use of the term "specially designed"

• Controlling printed boards by use of the term "specially designed" unnecessarily perpetuates longstanding confusion about the uniquely designed nature of all printed boards

Defense Cuts

• Maintaining a strong domestic printed board industry is critical to the nation's defense industrial base and national security

• Sustained federal budget reductions weaken the defense industrial base by undermining the solvency of a domestic supply chain responsible for America's 21st century military technologies

Executives attending from IPC member companies included: Steve Betza (corporate director of Advanced Manufacturing and Development, Lockheed Martin); Bob Black (president and CEO of Juki Automation Systems); Jack Calderon (managing director at Lincoln International

Figure 3: IPC executives voicing our views on key priorities in a meeting with Senator Mark Warner (D-VA).

Figure 4: IPC executives meet with Senator Rob Portman (R-OH) in the Capitol to press industry legislative priorities.

LLC); Everett Frank (vice president of Optimum Design); Dr. Brent Grazman (vice president of quality at Viasystems); Richard Lies (CEO of Chemcut Corporation); Jason Marsh (vice president for product management at Insulectro); Bhawnesh Mathur (president and CEO of Creation Technologies); Joe O'Neil (president of Hunter Technology Corp.); Marc Peo (president of Heller Industries); Carsten Salewski (CEO of Viscom Vision Technology); Ray Sharpe (president and CEO of Isola); Matt Turpin (president and CEO of Zentech Manufacturing); John Vaughan (president of Circuit Solutions LLC); Mikel Williams (president and CEO of JPS Industries); Mark Wolfe (director of supply chain management at John Deere Electronic Solutions); and Jim Woodbridge (vice president for government affairs, DoD Programs for SAIC).

The group meetings were followed by one-on-one meetings with representatives and their key staffers. This gave individual IPC member company executives the opportunity to meet with the offices of the representatives for their respective geographical locations and to provide more detail and granularity on our collective issues. The door is now open for many of us and the relationships that were formed can prove valuable, for both the member companies and the IPC, if properly nurtured over time.

"Every time I attend this event, I walk away with a renewed appreciation of the value of our government relations efforts," said John Mitchell, president and CEO of IPC. "Our meetings with senior leaders at the White House and on Capitol Hill give us a chance to educate them about our industry and the policies needed to maintain a strong electronics sector. We are grateful to the executives who attended and to the policy makers who met with us, and we will continue to work at growing these relationships and advocating for our industry."

From the two days filled with highlights, two stand out in my mind.

The first was our IPC Executive Luncheon with Rep. Bill Johnson (R-OH). Congressman Johnson made it easy to believe in America—

and in American manufacturing, again. He delivered an impassioned and patriotic keynote that touched upon the inner workings of the legislative body, the importance of electronics manufacturing to the United States, and the importance of both smart regulation and national security as it pertains to our industry. Congressman Johnson had us all ready to high five each other and run through brick walls. Thank you, sir.

Second was our closing meeting, held just off the West Wing of the White House in the Eisenhower Executive Office Building (EEOB) with Jason Miller, Special Assistant to the President for Manufacturing Policy. This meeting was special because of both the importance of the message we delivered and for the venue. Steeped in history, our meeting was held in the War Secretaries Suite of the EEOB. The IPC messaging detailing our support for the NNMI was delivered by IPC President John Mitchell and Steve Betza of Lockheed Martin. To date, four regional innovation hubs known as Institutes for Manufacturing Innovations (IMIs) have been launched, with Lockheed Martin as a tier one participant in all four. As Lockheed's corporate director of advanced manufacturing and development, Betza is extraordinarily well-versed on the topic and there was an excellent exchange of thoughts and ideas with Mr. Miller. There is an active request for information (RFI) to industry by the DoD. The purpose of the RFI is to solicit input from industry and academia that the DoD will consider as part of an effort to select and scope the technology focus area for future IMIs hubs. The DoD is requesting responses that will assist in the selection of a technology focus area from those currently under construction, based upon evidence of national security requirement, economic benefit, technical opportunity, relevance to industry, business case for sustainability and workforce challenge.

The technical focus areas currently under consideration are: flexible hybrid electronics, photonics, engineered nanomaterials, fiber textiles, electronic packaging and reliability, and aerospace composites.

To ensure the messaging that IPC delivered on Capitol Hill resounds in the future, IPC is also forming a political action committee (PAC). As outlined by John Hasselman, IPC's VP for government relations, "PACs have become an important tool for any group that wants to be heard when laws and regulations are written. Given the growing number of government regulations that influence the electronics supply chain, having a stronger voice in Washington, D.C. is something that can no longer be ignored."

IPC's PAC will support federal candidates for office that advocate for policies that support the growth of electronics manufacturing, and will help raise IPC's visibility with policy makers and other key influencers in Washington. As IPC continues to raise its profile, key members of Congress and administration officials are learning about the needs of our industry and the work IPC is doing. We need to continue to engage at a political and policy level and educate them on issues important to the success of our members. In a call to action, I would highly encourage IPC member company executives to consider participating in the PAC. For more detailed information about the PAC and other IPC's government relations activities, please contact Hasselmann at johnhasselmann@ipc.org.

In closing, IPC IMPACT 2014 was an outstanding event that provided each attendee with an insider view of the issues that impact our industry, our nation's political process, and IPC's extraordinary advocacy of our industries' position on these issues. IMPACT 2014 exceeded all of my expectations. The hope from here is that additional IPC member companies' executives will plan to attend next year's event and make a continued impact in Washington, DC on behalf of IPC members in the United States. **PCB**

John Vaughan is president of Circuit Solutions LLC, based in the Washington D.C. Metro Military market and providing integrated supply chain and program management solutions to the military C4ISR, Unmanned Systems and IED detect and defeat communities. To reach Vaughan, or to read past columns, click here.

PCB007 Supplier/New Product News Highlights

Panasonic Debuts Multilayer Circuit Board Material

Panasonic Corporation has developed MEGTRON 7, a multilayer circuit board material with the industry's lowest transmission loss, which meets the requirements for high-capacity and high-speed transmission of high-end servers, routers, etc., thereby contributing to the improvement of their signal processing performance.

Isola Hosts Rep. Mulvaney at South Carolina Facility

Congressman Mick Mulvaney (R-SC-5) visited the company's manufacturing facility in Ridgeway, to learn firsthand about policy and regulatory issues affecting the electronics manufacturing industry. He visited with Isola President Mike Gastonguay and discussed a variety of issues, including export controls, R&D tax credits, and intellectual property protection.

Rogers Expands in Arizona to Meet RO3000 Demand

Rogers Corporation's Advanced Circuit Materials Division has received board approval to install a RO3000 dielectric production line to increase capacity in Chandler, Arizona. Dielectric is a specialty polymeric substrate that is laminated at high temperature between two sheets of copper foil to create PCB material.

Ohmega Forms Process Support Group

Ohmega Technologies, Inc. is pleased to announce the creation of an OhmegaPly Process Support Group. The Group's charter is to lend technical and logistical support for PCB shops interested in processing OhmegaPly embedded resistive technology.

Park Electrochemical Sees Drop in Q4 Results

Park Electrochemical Corporation reported net sales of $38,151,000 for the fourth quarter ended March 2, 2014 compared to net sales of $42,675,000 for the fourth quarter ended March 3, 2013.

Gardien Services USA Debuts A8/G60 Test Combo

Gardien Services USA is happy to announce the addition of its new Acceler8/G60 Flying Probe combination to its ever expanding Quality Assurance offerings available in Plymouth Minnesota.

SOMACIS Launches Zeta Cap Material

Zeta Cap is a copper-clad, high T_g glass-free laminate, produced by Integral Technology and designed to eliminate pad cratering, a serious and evolving challenge for the PCB industry.

Uyemura to Provide Solutions to eSurface Licensees

eSurface Technologies, the developer of the eSurface manufacturing process for PCBs, has confirmed that Uyemura, USA, has become an eSurface Certified Supplier, effective immediately. Uyemura will support the eSurface licensee's needs for products in the facilitation of the eSurface process.

ETI Visits Asian Market; Expands Customer Base

Equipment Technologies Inc. (ETI) continues to expand its customer base with more site visits in the Asian market. Eric Winkler, international VP of Marketing and Sales for ETI, was given onsite access for inspection of multiple shops current processes to suggest various upgrades to increase efficiency.

LPKF's LDS Powder Paint for Metal Substrates

Since the LPKF LDS PowderCoating was first announced in fall 2013, developers have expressed interest in using it in a multitude of applications. New product layout possibilities are opened up for producers of LED lights with the LDS powder coating, which enables any spatial arrangement of LEDs and offers good thermal properties.

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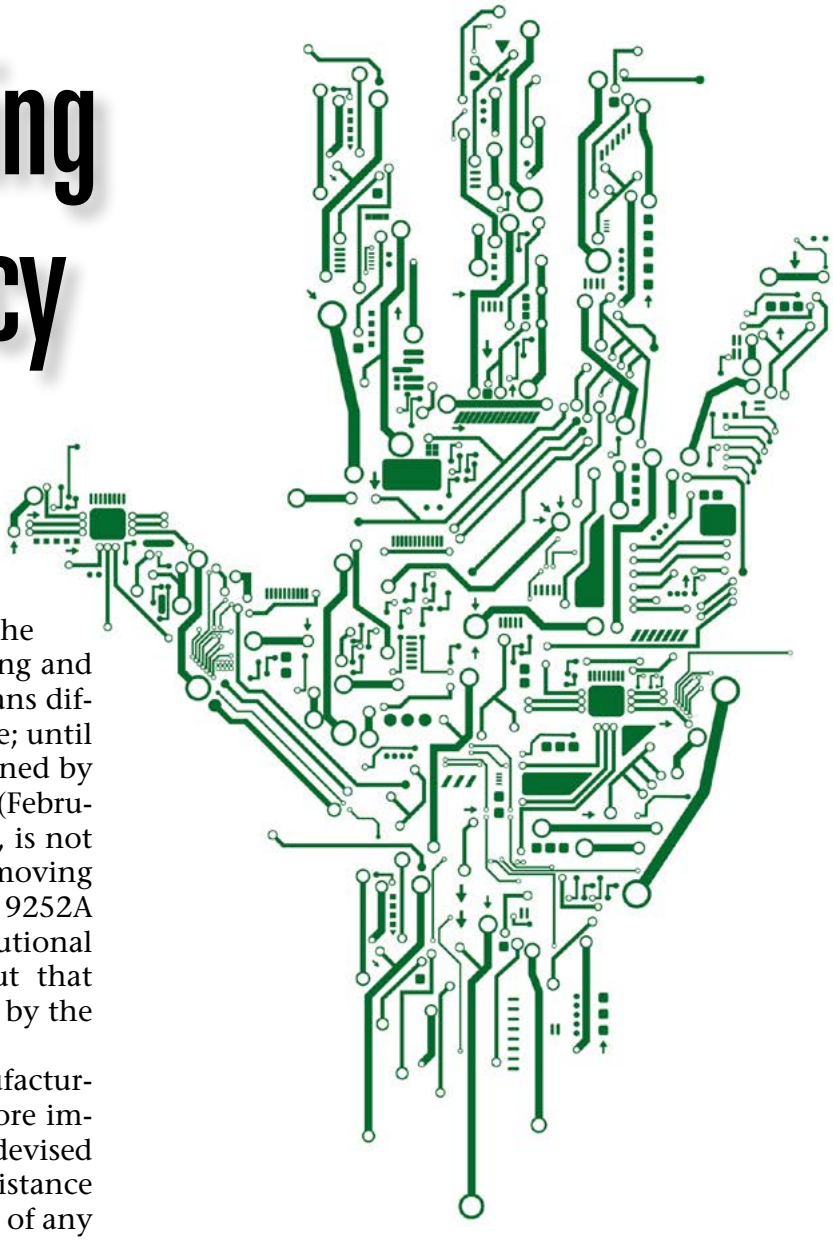
Isolation Testing and Adjacency

by Rick Kaim
ALLY SUPPLY INC



Whether you have a cursory understanding of adjacency or the subject is new to you, this article will explain the past and current state of adjacency testing and where it is heading. Why adjacency means different things to different people is simple; until recently it had not been adequately defined by an industry standard body. IPC- 9252 (February 2001) section 3.1, Adjacent Features, is not an explanation of adjacency used by moving probe technology. The next revision of 9252A did address adjacency and set an institutional minimum standard; important yes, but that does not guarantee a full understanding by the industry, and most importantly, users.

Until recently, moving probe manufacturers have set their own standards and more importantly CAM software providers have devised their own best methods. Adjacency distance value (ADV) is the distance from an edge of any feature on one net to an edge of any feature on another net.

The proper ADV is important to many stake holders, from prober equipment manufacturers and the CAM software suppliers, to the board shops, their customers and finally, the end-users. None of these entities are myopic; for instance, a board shop has both a quality manager and a production manager, but these are opposing forces in the world of adjacency. What is the best compromise for end-users and board manufactures?

Let's look at adjacency's past, present, and likely, future. What adjacency has done in its past is truly remarkable; it has allowed flying probes testers to enter the mainstream of bare board electrical test. By using logic to overcome a physical limitation, a new industry within an industry was born. The other major influence in mainstreaming probers was signature (capacitance) testing, which is a separate subject from adjacency.

The basic need was to tackle isolation iteration explosion. If each net was tested against all others the number of tests is [N x (N-1)]/2. So, for example (Figure 1).

It is easy to see that a small number of nets can be tested completely, but a larger number of nets become unrealistic; even if a prober could test consistently at 10K test points per minute (and none can) the isolation test on the 10K net board would take more than 80 hours! Probers on average can test isolation in the hundreds of nets per minute, not thousands, in resistance mode because of the X, Y and Z motion need before the test can occur. The X and Y motion

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September 18 & 19, 2014

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INEMI, MEPTEC, and SMTA have joined forces to host this international conference, focusing on advances in electronic technologies and advanced manufacturing, specifically targeting medical and bioscience applications. Previously, MEPTEC's and SMTA's conferences were held in Phoenix, Arizona and Milpitas, CA, respectively, drawing technology experts, entrepreneurs and service providers that work in this niche technology space. Typical applications within this space involve implantable defibrillators, neurostimulators and drug delivery, interventional catheters, pillcams, ultrasound transducers, hearing aids, biosensors, microfluidics, wireless communications, as well as future diagnostic and treatment solutions that may use stretchable electronics, microelectromechanical systems (MEMS) or nanoelectromechanical systems (NEMS). ◆

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Multiple Track Topics Include:

Track 1:
Components and Designs for Higher Density Functionalities

This track will focus on advances in electronics components and designs that can make current medical electronics ever more miniaturized with more functionality and at lower power.

Track 2:
Solutions for Best-in-Class Assembly and Volume Manufacturing

This track will focus on critical methods and protocols to ensure that the production of Class II and III medical electronics is conducted in the most effective, efficient and quality-controlled way with full traceability and zero defects.

Track 3:
Next Generation Microelectronics for Changing Healthcare Markets

This track will focus on advances in next generation, revolutionary microelectronics for medical devices and applications that solve technology challenges and are aligned with solutions for new healthcare models.

KEYNOTES

Digital Health and the Connected Consumer

Matthew Hudes
U.S. Managing Principal, Biotechnology
Deloitte Health Sciences

What Can Medical Devices Leverage from Consumer Electronics?

Chandra Subramaniam
Vice President CRDM Research & Development
Medtronic

Ensuring Quality Medical Devices Meet Regulatory Scrutiny in the Face of Industry Cost Pressures

Mike Tendick
Healthcare/Life Sciences Market Sector Vice President
Plexus

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is dictated by the board layout and the Z by the flatness when tested. Note, as test voltage goes up time also is needed to create then discharge it increases so test time also increases especially above 250V.

Because moving probe testers do not contact all testing points at the same time the motion of the probes to the testing points governs the test time and therefore cost. Isolation testing takes considerably more combined moves than continuity testing and therefore is the major consideration in total test time.

ADV is a distance that is used in software applications to determine which nets will be tested against each other for isolation. The basic logic is if two nets are never expected to short against each other the test can be eliminated (i.e., two small nets on opposite sides of the board separated by several inches). Net combinations that have a potential to short to each other should be tested. ADV is used to divide the tested from the non-tested net combinations. The first and most basic use of the method simply uses a distance between features to determine the list. If any feature of a net came within the chosen distance from a feature on another net the two were tested against each other for a short.

Nets	Isolation Tests
2	1
3	3
4	6
5	10
10	45
100	4,950
200	19,900
300	44,950
500	124,750
1000	499,500
10,000	49,995,000

Figure 1: Examples of isolation test vs. number of nets.

Line of sight added some logic to the previous method by further analyzing the set of tested nets to see if some of the tests could be eliminated. The logic was if two nets were to be tested against each other but the results could be known by analyzing other tests that test could be eliminated. In physical terms, if two nets can't be shorted without shorting to an intermediate net (straight line) then the test is eliminated and the intermediate tests are used to guarantee the test integrity.

Line of sight can be a safer test if the adjacency distance is increased. The total number of tests is not increased by the previous formula because the tests have been eliminated that would be detected by other shorts tests.

Through-hole spacing is generally greater than surface mount spacing per device but both are commonly on the same board. Many boards have a mix of the two, so the larger value should be chosen. The test takes longer than it would for the surface mount features because a smaller ADV would have been chosen if the through-hole devices were not on the board. A major advancement in choosing the proper adjacency value would be to separate the distances into different categories, such as: through-hole, surface mount, single point nets, user-defined points per net (nets with 10 endpoints or less), trace width (nets with trace width larger than 20 mills). To have a minimum number of tests per net a net must be tested against two other nets.

Currently the ADV is chosen then the CAM software develops the list of isolation tests and the programmer is made aware of the number of tests. This information can be used to judge the initial value chosen and this can be an iterative process. In practice, the process is rarely repeated. The logical place for a rigorous evaluation is in the test extraction software. Because printed circuit boards are unique, it isn't possible to choose a single adjacency distance for all boards. There is no simple formula that can cover all possibilities; only through software analysis can the best value can be achieved. Evolving software tools need to be vetted and ongoing feedback to the IPC subcommittee on electrical test is in the best interest of all stakeholders. **PCB**

Rick Kaim is the president of Ally Supply Inc. To contact the author, click here.

Why Removing Your Bottleneck is a Bad Idea

by Gray McQuarrie
GRAYROCK & ASSOCIATES

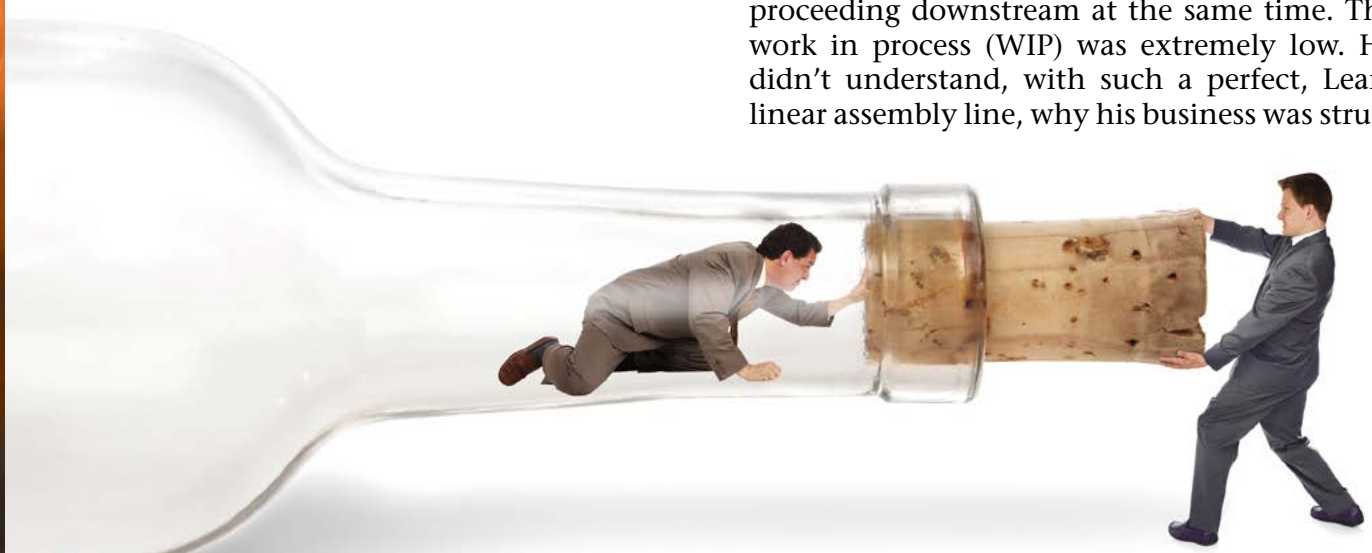
I received a number of comments about my column, Are Boringly Predictable Operations Possible? (February 2014). An argument repeated to me again and again was, "We don't have a capacity problem! We have a sales problem! I have plenty of capacity!" To which I think, but do not say, "No you don't, otherwise you wouldn't have a sales problem."

Let me give you an example. Let's say you have one LDI machine for building your HDI product. This machine is only utilized 40% of the time. The orders coming off this machine generate 80% of your profits. You would tell me, "Gray, we do not have a capacity problem at LDI." And I would likely be unable to convince you otherwise. Let's say you have a number of orders going through your shop that are not only HDI, but HDI quick-turn premium orders. If you complete these orders on time you will have revenue and profitability numbers for the month that will be record breakers. Then the LDI machine suddenly goes down. You have zero throughput for a week as the machine is repaired. This lack of a second machine, this extra capacity, is going to have a negative impact on your current and future sales.

You could say that isn't what you meant about not having a capacity problem—of course having only one machine for doing critical work is risky. Then why did you let the Lean expert strip you of all excess capacity in order to level load and balance the production line if you knew intuitively this would increase your risk? On a recent internet search, I found this: "Line balancing is leveling the workload across all processes in a cell or value stream to remove bottlenecks and excess capacity." The article stated, "Match the production rate after all wastes have been removed to the takt time at each process of the value stream."

This is a very popular, yet insane thing to do.

Some years ago I got into a discussion with a CEO about process bottlenecks. He asked what happens if you don't have any bottlenecks, because his operation didn't have one. I was speechless. The process that defined his business (it wasn't PCBs, but it is related to a popular chip assembly option) had several machines where one machine fed another and then another in a connected one-piece flow, where a single job couldn't break the chain, with no extra machines in parallel, and with everything proceeding downstream at the same time. The work in process (WIP) was extremely low. He didn't understand, with such a perfect, Lean, linear assembly line, why his business was strug-



Designers: when you choose a fabricator, what guarantee do you have that they won't deliver scrap?

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gling with wildly fluctuating revenue and unexpected missed delivery dates. He was vexed.

Here is the reality. Think of a hose. Does it have a bottleneck? Yes, its entire length is a bottleneck. Can you remove it? Yes, with the result being water shooting out of the spout. Can this bottleneck be removed? Yes, with disastrous results. Even when you get to the giant aquifer or reservoir you have not removed the bottleneck; the capacity is much greater so your constraint on flow is at a much higher rate of flow, but there is still a constraint somewhere. There is always a bottleneck.

Let's get back to the CEO who thinks he doesn't have a bottleneck. A great way to understand his situation is from an example called Penny Fab 1, from the landmark textbook, Factory Physics®, by Mark Spearman and Wally Hopp. Here you have four work stations to make a penny: punch, stamp, rim, and deburr. And let's say each station takes two hours to complete with no variation. Figure 1 shows the plant layout for the discrete event model. I am not going to go through the detail of explaining that the critical WIP for this scenario is four pennies, that the total process time is eight hours, and the bottleneck rate (where each station is the bottleneck) is 0.5 pennies per hour.

In Figure 2, the blue line shows how the throughput changes with WIP (left scale). This is the "best case" scenario for throughput. It is impossible to have throughput better than

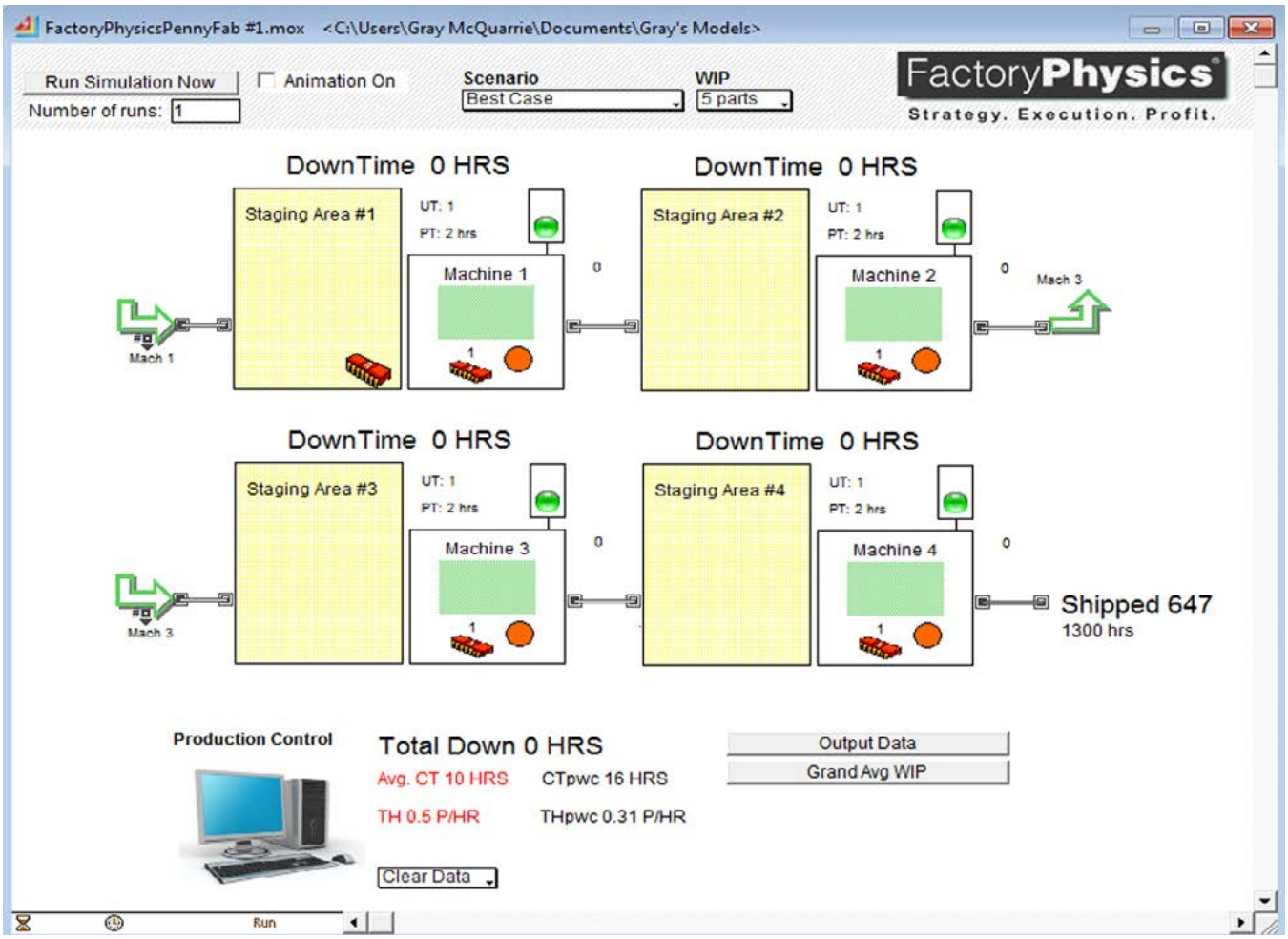

Figure 1: The result of running the simulation for 1300 hours at a WIP level of 5. Each station was 100% utilized with a process time of two hours per machine. The "best case" scenario is impossible to achieve.

(above) this blue line. The reason why the critical WIP is four is because this is the point that the maximum theoretical throughput with zero variability is attained.

The purple line represents the best case scenario for cycle time, which is defined as the total process time plus the total wait time, which is the total time it takes a penny to travel through the entire process. It is impossible to have a cycle time that is better (below) the purple line.

Is the "best case" bottleneck rate and "best case" cycle time ever achievable in reality? It is not, because of variability. One way to understand this inefficiency is to imagine a freeway completely packed with cars touching. Nothing is going to move! Having cars touching can only happen if all the cars are going at a 0 velocity with no variation (which is a long-winded way to explain parked cars). This would be the case even if you slipped the transmission from park to drive and slammed down on the accelerator. Lots of burnt rubber, but no movement. In order to move we have to have some space between the cars (a buffer); therefore, the number of cars per minute that pass under a bridge is going to be less than the theoretical number of cars that could pass under the bridge if we could all drive at exactly 55 mph.

Mark Spearman and Wally Hopp derived a marginal case in order to evaluate the goodness of a specific production system. In Figure 2, the marginal case for throughput is the red line and

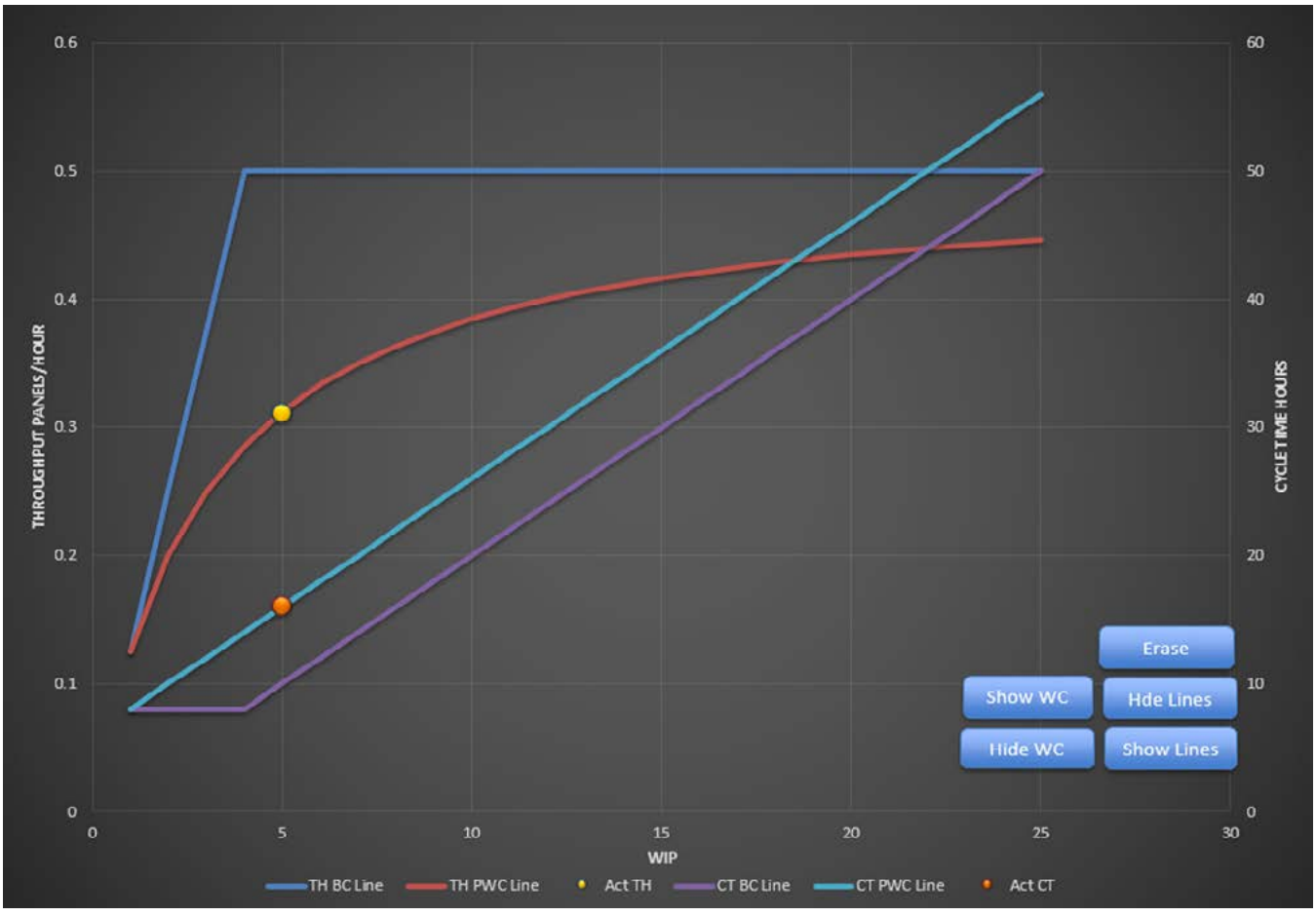

Figure 2: Comparison of the best and marginal cases for throughput and cycle time, with two plots for throughput where the scale is on the left and two plots for cycle time where the scale is on the right. In order to improve significantly over the marginal case (red line for throughput and cyan line for cycle time) you have to do things that go against Lean such as unbalancing the line and/or adding capacity.

the marginal case for cycle time is the cyan line. I show the result of running the simulation with a WIP of 5. The yellow dot is the marginal throughput and the orange dot is the marginal cycle time. With the marginal case, all process times must be the same, the variation must be exponentially distributed, and there is no passing of product.

There are specific formulas that describe the resulting marginal case curves in Figure 2[1].

By the way, this marginal case should remind you of the balanced production line for the CEO described above.

What does this graph mean? If your actual performance is below the marginal case line for throughput, chances are you can improve your performance simply by reducing the variation in your process times or improving the variation in your up time on your machines. If your performance is at or better then the marginal case line, then improving your performance may be difficult and you may have to make systemic changes to your manufacturing operation (e.g., add machines or people).

Consider the impact we have experienced by reducing our lot sizes. What industry has done in decreasing lot sizes is to significantly reduce average cycle times. This is a good thing, but it has unintended consequences. What the industry in general does not realize is that too little WIP is as bad as too much WIP. As the curves above show, decreasing WIP decreases cycle time but it also decrease throughput. Here is where managers go astray. They love the shorter

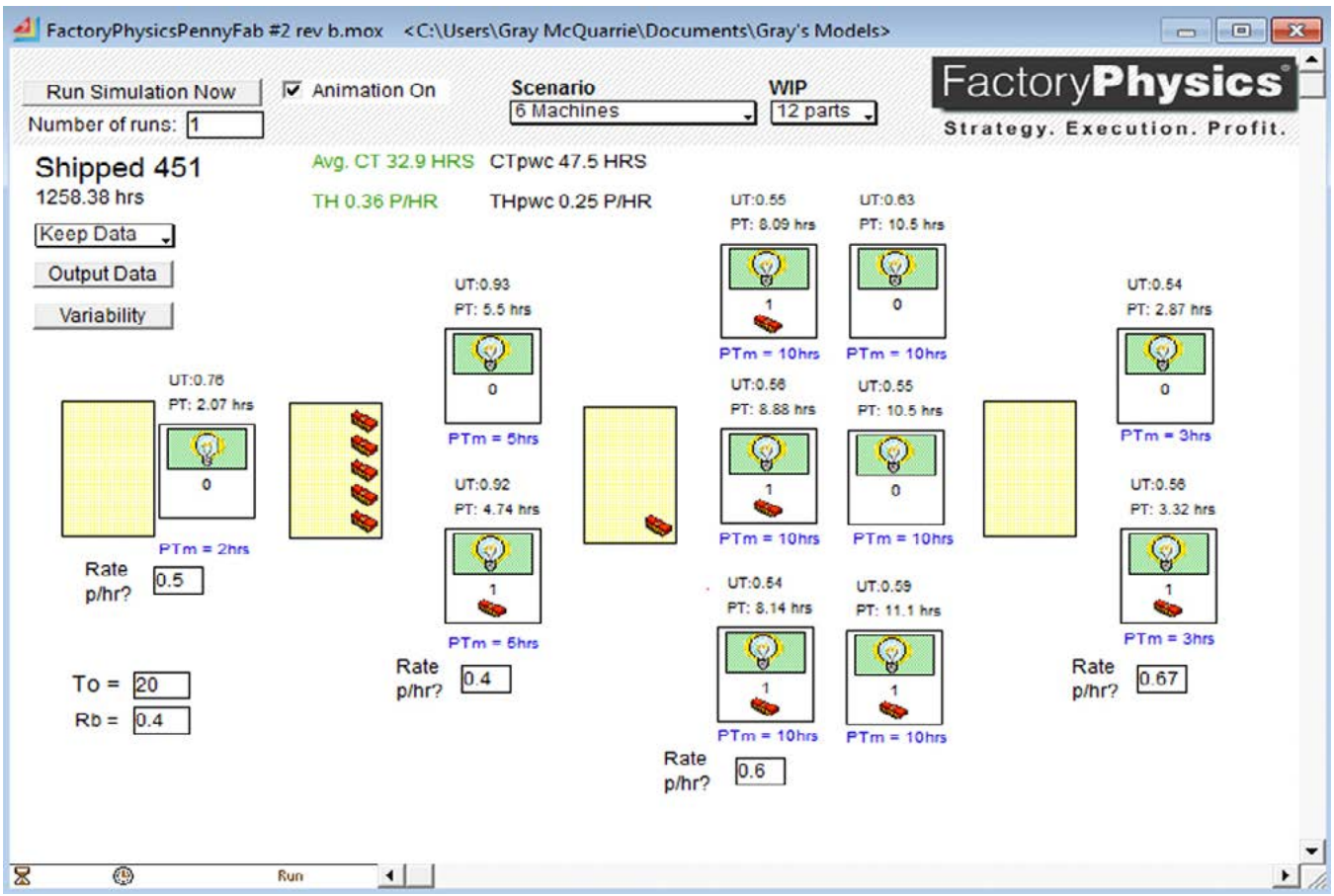

Figure 3: An unbalanced production line with plenty of capacity. Note the second department with two machines has a utilization of over 90%, but the utilizations downstream of the bottleneck are only slightly above 50%. Unbalanced lines tend to keep the bottleneck fed and prevent the bottleneck from being blocked.

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cycle time, yet they lose sight of the fact that the reduced amount of WIP does not provide enough buffer for the variability in their processes. The result is that the bottleneck starves frequently and total demand can't be met. So any one order can be completed very quickly yet there is not enough volume in output to satisfy all demand. The unintended consequence of this is that mangers start expediting most orders depending on the latest, hottest fire. This in turn:

- Increases product mix, which
- Accelerates the shifting of bottlenecks, which
- Makes production management much more difficult and
- Increases the variability in cycle time, which
- Makes customer service worse, which
- Leads to more expediting and the downward merciless cycle of ruination

Figure 3 shows an unbalanced scenario from Factory Physics called Penny Fab II. Here we have one station taking two hours to punch, two stations taking five hours per machine to stamp, six stations taking 10 hours per machine to rim, and two stations taking three hours to deburr. I am not going to provide a detailed explanation on the fact that the total process time is 20 hours, or that the bottleneck rate is at station two and is 0.4 parts/hr, and the critical WIP is only eight parts in this system. It should be obvious that this isn't a balanced production operation.

Figure 4 shows the result of the throughput and cycle time as compared to the marginal case (the case where it would be single machines at each station, all operating at the same speed, with no passing allowed: the ideal case for level

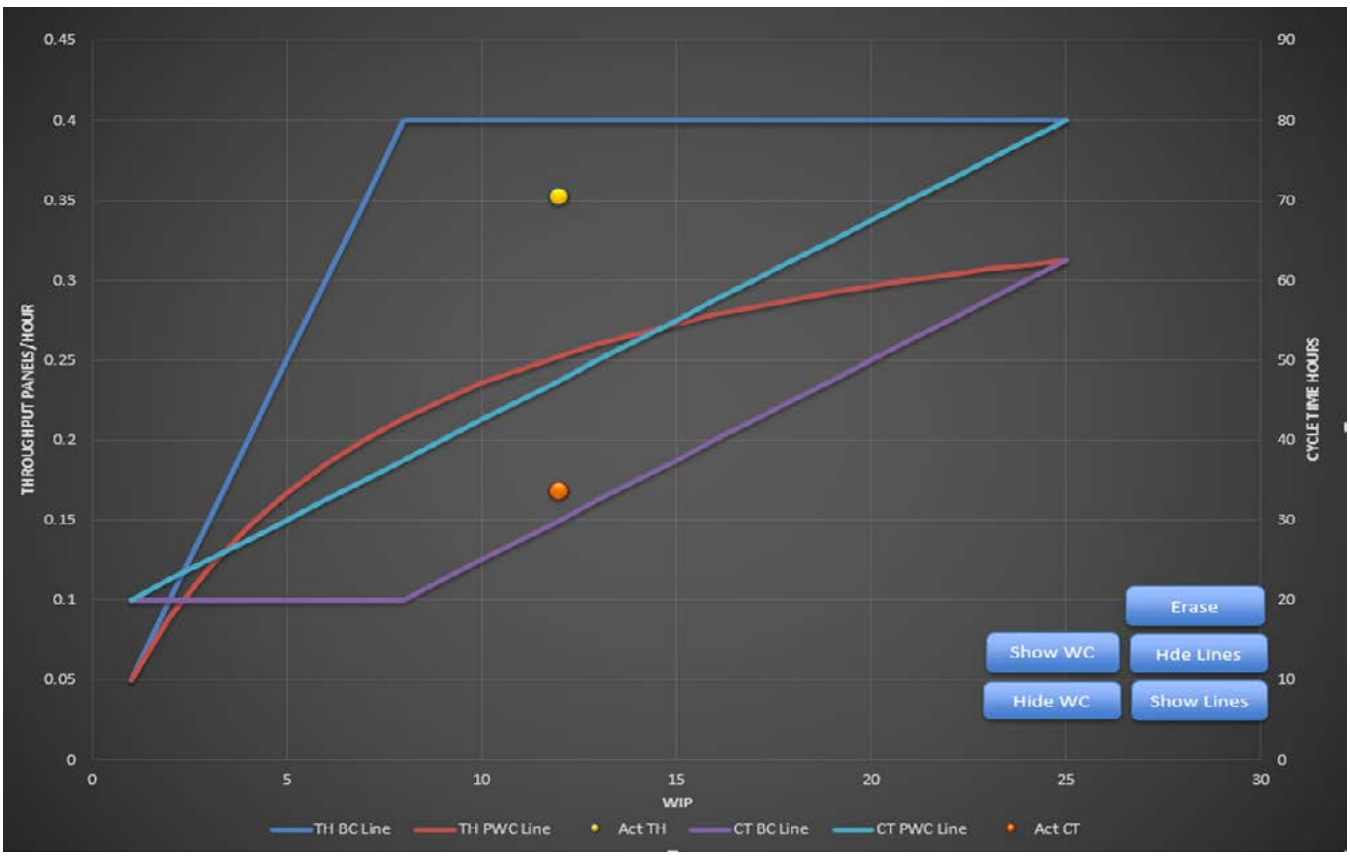

Figure 4: The superior performance gained by having too much capacity with a substantially improved throughput and cycle time over the marginal case. In the real world you have to decide if this extra performance is worth the investment in the additional capacity.

line loading and balanced production). The result over the marginal case is huge! Why? Product being able to pass slower moving product is a good thing, not a bad thing! For example, imagine what it would be like on a freeway where once you entered you weren't allowed to pass any cars! Imagine what would happen if granny was driving on the road! Similarly, if one machine is taking longer than another to process, the next machine available can be chosen. The question is how many machines and extra capacity do you need? This is a sophisticated problem that involves tradeoffs and diminishing returns. For example, the more expensive the machine then the more difficult it is to justify adding more capacity.

What does this all mean for us in our shops? A year ago, I wrote, What is the DAM Problem with Scheduling (July, 2013). It blows up into an NP Hard problem (an impossible to solve problem with today's computing technology) as you increase the number of bottlenecks in the plant. One possible way to not only improve your plant's performance for throughput and cycle time is to add extra capacity, which would create a capacity buffer, and to do this in such a way that you have a well-defined bottleneck in your factory no matter the product mix. This might be too expensive or too idealistic to achieve, but it is well worth thinking about. **PCB**

References

1. Factory Physics. Hopp, Wallace J., and Spearman, Mark L. (3rd edition, 2008, McGraw Hill: New York).

Gray McQuarrie is president of Grayrock & Associates, a team of experts dedicated to building collaborative team environments that make companies maximally effective. To read past columns, or to contact McQuarrie, click here.

VIDEO INTERVIEW

ETI/NEA: Combining Expertise through Merger

by Real Time with...IPC APEX EXPO 2014

Guest Editor Kelly Dack chats with ETI/NEA President, Jon Pelletier, who explains the companies' merger and specializations within the industry.

CLICK TO VIEW

realtimewith.com

Mil/Aero007 News Highlights

Dragon Circuits Adds Up-cycled PCBs to Drone Division

Since Dragon started their UAV/drone branch earlier this year, the first step to up-cycle scrap material for drones was an obvious one. Vice President Rajan Babaria comments, "Many circuit boards are layered and quite durable. It was clear this would make them a great candidate to be used as a drone frame."

IPC Offers One-day Conflict Minerals Conference

Continuing its long-standing conflict minerals educational outreach efforts, IPC is offering a one-day conference, "Conflict Minerals: Staying Current in a Changing Landscape," July 10, 2014, in Santa Clara, California to provide manufacturers up-to-the-minute information on the changing landscape of conflict minerals.

Invotec's Flex Rigid PCBs Earn ESA Approval

Having secured its first approval from the European Space Agency (ESA) earlier this year, Invotec Group is delighted to announce that it has now gained approval for sequential flex rigid boards.

i3 Electronics to Supply PCBs for Satellite Use

The company announced that an industry-leading aerospace and telecommunications firm has awarded the company a substantial contract for the supply of its high-complexity, high-reliability PCBs for a satellite application.

Gardien Services USA Debuts A8/G60 Test Combo

Gardien Services USA is happy to announce the addition of its new Acceler8/G60 Flying Probe combination to its ever expanding Quality Assurance offerings available in Plymouth, Minnesota.

FTG Secures LTA for PCBs for Wing Platforms Use

Firan Technology Group Corporation has been awarded a new three year long term agreement (LTA) from one of the leading global OEMs supporting the aerospace market. The agreement incorporates a variety of high-technology PCBs for use on key fixed-wing platforms including the Boeing 787, Airbus A350, A400M, and the Bombardier C-Series.

Ventec Europe Announces AS9100 Rev C Accreditation

The company is proud to announce that the quality management system at its Leamington Spa, UK, headquarters is now fully accredited to AS9100 Revision C, in accordance with the Aerospace Supplier Quality System Certification Scheme EN9101:2011, EN9104-001:2013.

Possible Expansion of Anti-counterfeiting Efforts

Applied DNA Sciences' SigNature DNA marking program is currently in use by several defense industry suppliers for application on electronics deemed to be at high risk for counterfeiting. A House committee has begun consideration of the DoD's fiscal year 2015 budget request, taking particular interest in efforts to combat the intrusion of counterfeit parts into the military supply chain.

SIA Lauds DoD Rule Reducing Counterfeit Semicon

The Semiconductor Industry Association (SIA), representing U.S. leadership in semiconductor manufacturing and design, has applauded a newly finalized DoD rule that reduces the risk of counterfeit semiconductor products being used by our military by implementing needed safeguards in the procurement of semiconductors and other electronic parts.

Aerospace & Military APU Market to Hit CAGR of 3.92%

APU use the same fuel as the aircraft's engines and generally account for about 2% of the total fuel consumption on a given mission. The global aerospace and military APU market is estimated to be $1,527.89 million in 2014 and is projected to register a CAGR of 3.92% to reach $1,851.69 million by 2019.

Delivering the highest quality standard for Aerospace and Defense

Ventec Europe Accredited to AS9100 Revision C

We are proud to announce that the quality management system at our Leamington Spa, UK, headquarters is now fully accredited to AS9100 Revision C (the two facilities of our parent company, Ventec Electronics Suzhou Co Ltd, have been fully AS9100C certified since 2012).

AS9100 is the quality management standard specifically written for the aerospace and defence industry, to satisfy authorities such as the Federal Aviation Administration, ensuring quality and safety in the "high risk" aerospace industry.

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Oxide Alternative Processes: Performance Characteristics

by Michael Carano
OMG ELECTRONIC CHEMICALS

Introduction

It is all about optimizing the performance of the oxide alternative chemistry. This includes close monitoring of the main reactive ingredients of the process chemistry. And one of the first issues that the industry had to address, whether one is using reduced oxide chemistry or oxide alternatives, is pink ring. While the industry has enjoyed moderate success at minimizing the dreaded pink ring defect with reduced oxides, the desire has long been to simplify the bonding treatment process. Secondly, improving bond strength on high-performance and advanced resin materials is critical to the successful implementation of any interlayer treatment process. While the latter attribute is well documented, the ability of the oxide alternative bonding system to resist pink ring must be established. In all instances, where multilayer PWB test coupons (some fabricated with reduced oxide, others with alternative bonding treatment) were subjected a severe acid test, no pink ring was detected. The coupons were immersed in an aqueous solution of 17% hydrochloric acid for 15 minutes. After removal, the coupons were horizontally ground down to remove the outerlayer pad. Coupons were then inspected under 30x microscope. No pink ring was detected on the coupons fabricated with the organo-metallic (oxide alternative) bonding process. However, the reduced oxide bonding process showed pink ring (Figures 1 and 2).

It is important to recognize that the existence of pink ring does not suggest that the PCBs are rejectable. In fact, pink ring is defined in the IPC-600H (acceptability of printed circuit boards) as a process indicator. No evidence exists that pink ring affects functionality. In fact, the presence of pink ring concerns a number of manufacturing processes. The focus of concern should be the quality of the lamination bond, the laminate materials, drilling, desmear metallization processes. As an example (Figure 3), etchback prior to metallization can open up a

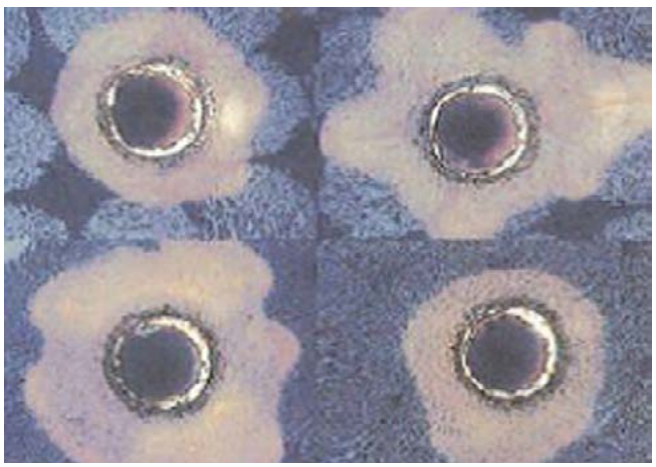


Figure 1: Reduced oxide coupons showing pink ring.

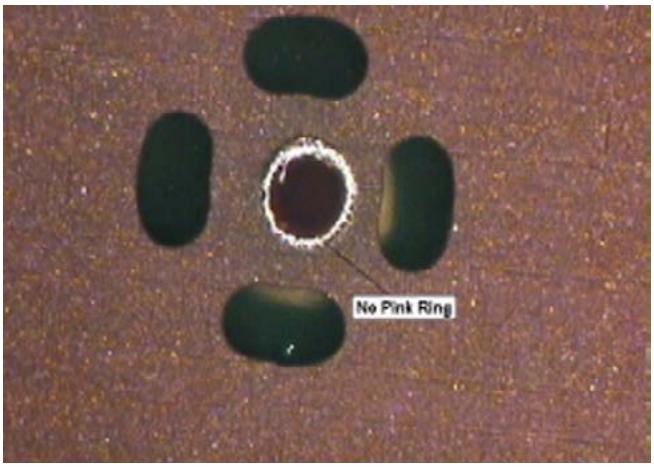


Figure 2: Organo-metallic process for MLB coupons; no pink ring found.

SAVE THE DATES!

Upcoming IPC Events

July 10
Conflict Minerals: Staying Current in a Changing Landscape
Santa Clara, CA, USA

August 20
Southeast Asia High Reliability Conference
Penang, Malaysia

September 23–25
IPC India Conference & Workshops
at electronica & productronica India 2014
Bangalore, India

September 28–October 2
IPC Fall Standards Development Committee Meetings
co-located with SMTA International
Rosemont, IL, USA

October 14–15
IPC Europe High Reliability Forum
Düsseldorf, Germany

October 28–30
IPC TechSummit™
Raleigh, NC, USA

November 18–20
High-Reliability Cleaning and Conformal Coating Conference
sponsored by IPC and SMTA
Schaumburg, IL, USA

November 19
Assembly & Reliability Conference
Bangkok, Thailand

December 3–5
International Printed Circuit and APEX South China Fair
(HKPCA and IPC Show)
Shenzhen, China

More Information
www.ipc.org/events

Questions? Contact IPC registration staff at +1 847-597-2861 or registration@ipc.org.

Strengthening & Advancing Electronics Manufacturing Globally

wedge between the B-stage material and the oxide (or oxide alternative). The wedge defect thus can act as a via allowing acid chemicals to seep in, removing some of the treated copper foil coating leading to the appearance of pink ring.

Stay tuned for more on these manufacturing interactions in a future column.

Process Flow

the alternative bonding process is easily implemented as an immersion system or in horizontal conveyorized mode. Equipment considerations are minimal and capital expenditure is within the realm of the majority of pwb fabricators. Let's look at a more detailed view of the process flow:

The recommended process flows and dwell times for the immersion (vertical) and horizontal (conveyorized) processes are listed below:

	Immersion	Horizontal
Acid Cleaner	180 sec	30 sec
Rinse	60 sec	45 sec
Pre-dip	60 sec	45 sec
Coating step	60 sec	40 sec
Rinse	60 sec	20 sec
Dry	300 sec	30 sec

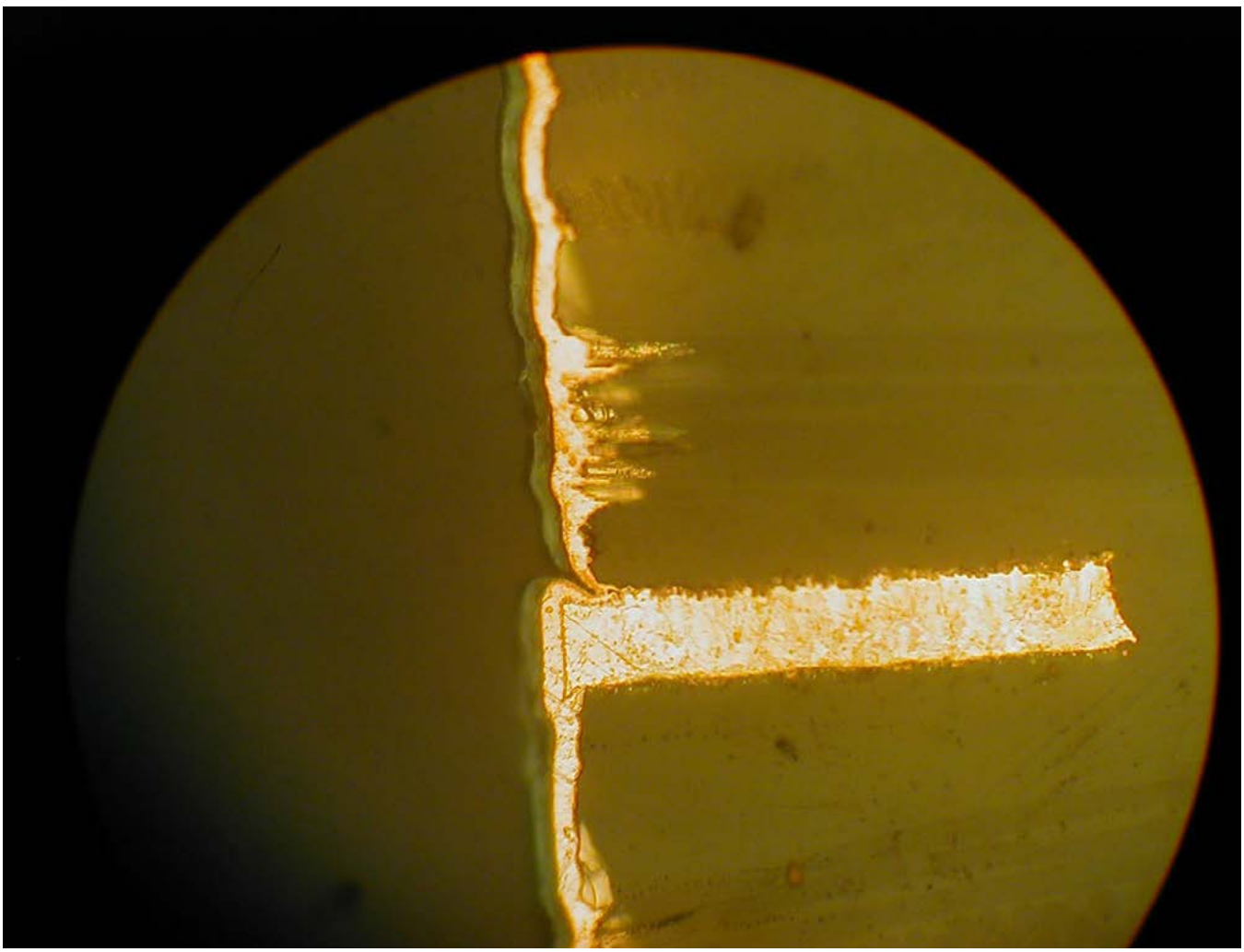


Figure 3: Etchback leading to wedge between pre-preg B stage and treated copper foil.

One should note how quickly and efficiently the process flows. The organo-metallic coating (formed in the coating step above) is formed very quickly. The organo-metallic bonding process provides much greater through put than reduced oxide processes.

Process Control

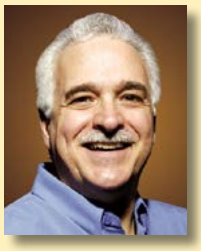
The organo-metallic bonding process offers advantages over standard oxide processes in terms of consistency and ease of control. Replenishment of the organo-metallic bonding solution is usually done with a "feed and bleed" system. Typically components are pre-mixed in a side tank and then replenished based upon a panel counter, a copper sensor or a specific gravity controller.

Each of the control methods has its advantages and disadvantages. A panel counter is easy to use and involves little maintenance but it does not accurately track copper build up in the bath when panel size and percentage of copper area vary widely. A copper sensor measures copper concentration by determining the amount of light that can pass through the solution. Due to the organo-metallic complex that is formed the etching solution may foul the light sensor resulting in the need for more frequent maintenance of the probe. The specific gravity controller measures the specific gravity of the solution, which is influenced by all of the components as well as copper concentration. If the bath components are controlled within a consistent range then specific gravity is a good indicator of copper concentration. If the bath components, especially sulfuric acid, are not controlled within the proper limits, then the specific gravity controller will not accurately control copper concentration. Despite the drawbacks of the control methods all three of the methods have been used successfully in field applications.

As an added benefit, the concentration of all major components of the alternative bonding bath can be analyzed using simple analytical procedures. This minimizes performance problems by ensuring the bath components are properly balanced. Proper balance of the components is necessary so that appearance, bond strength and resistance to thermal excursions are all acceptable. This is especially critical when using high-performance resin systems such as high T_g FR-4, polyimide and PPO.

Summary

Achieving optimum performance with oxide alternatives depends on many factors including material selection, lamination parameters and process control of the key additives that make-up the system. At the very least process engineers must consider specific gravity as one method to maintain the copper concentration in the working oxide alternative solution. **PCB**



Michael Carano is with OMG Electronic Chemicals, a developer and provider of processes and materials for the electronics industry supply chain. To read past columns, or to contact the author, click here.

New Hybrid Circuit Could Take the Place of Silicon

Researchers from the USC Viterbi School of Engineering describe how they have overcome a major issue in carbon nanotube technology by developing a flexible, energy-efficient hybrid circuit combining carbon nanotube thin film transistors with other thin film transistors. This hybrid could take the place of silicon as the traditional transistor material used in electronic chips, since carbon nanotubes are more transparent, flexible, and can be processed at a lower cost. Electrical engineering professor Dr. Chongwu Zhou and his team developed this energy-efficient circuit by integrating carbon nanotube (CNT) thin film transistors (TFT) with thin film transistors comprised of indium, gallium and zinc oxide (IGZO).

"I came up with this concept in January 2013," said Dr. Chongwu Zhou. "Before then, we were working hard to try to turn carbon nanotubes into n-type transistors. Instead of forcing nanotubes to do something that they are not good for, we found another ideal material for n-type transistors—IGZO."

TOP TEN

PCB007 News Highlights This Month

1 North American PCB Industry Growth Still Slow

"With year-to-date growth rates improving but still negative, and a book-to-bill ratio just barely in positive territory for the second month, the North American PCB industry appears to be moving very slowly toward a modest recovery this year," said Sharon Starr, IPC's director of market research. "The negative month-to-month growth rates in April reflect normal seasonal patterns."

2 IPC PCQRR Database Allows PCB Fabricator Comparison

The IPC Printed Board Process Capability, Quality, and Relative Reliability (PCQRR) Database was developed by IPC and Conductor Analysis Technologies Inc. in 2001 for designers, purchasers, assemblers, and manufacturers of PCBs. It gives board buyers a way to compare board fabricators, and fabricators a way to compare their processes to the industry at large.

3 Invotec Strengthens Euro Team with New Appointments

Invotec Group is delighted to announce the appointment of Thomas Witt and Monika Braun as sales agent and sales assistant for Germany. Witt joins the company with extensive experience as a sales account manager, primarily within the high-reliability PCB sector, whilst Braun has a strong customer service background in the PCB industry with a particular focus on quick turnaround orders.

4 Candor Highlights Cutting-edge PCB Manufacturing

Candor President Yogen Patel remarks, "We're extremely excited over the success we've had achieving these high-end, technical builds. With the speed at which the industry changes these days, Candor wants to be ahead of the pack, at the forefront of technology.

5 FPCB Report: Mektron Suffers First Loss

The world's largest FPCB company, Mektron, suffered its first loss since its establishment, due to three main reasons: HDD and ODD markets contracted; the company began to intervene in the price war; and the company's 45% output came from China where RMB appreciation and rising labor costs eroded profits.

6 Multiline Restructures Business; Sharpens Focus

Multiline Technology has restructured its business to improve consistency and dependability while delivering custom equipment and spare parts. In the last few years, the company's business has changed to comprise predominately multiple camera, very tight tolerance, and large format post etch punches.

7 NCAB Expands U.S. Presence, Acquires M-Wave

One of the world's largest suppliers of PCBs, NCAB Group, has acquired 100% of M-Wave International LLC's PCB Division. Bob Duke, former president of M-Wave's PCB Division, commented, "Being selected by NCAB to be a part of their U.S. team is a great compliment. As the PCB supply market continues to evolve, I felt this was an excellent time for M-Wave to expand its resources."

8 Matrix Opens New "Value-added" California Warehouse

Branch Manager Jim Alves reports that the new warehouse is now in full operation. With the ongoing success of Panasonic High-Speed laminates, Jinzhou Carbide Tools, and Agfa Specialty products, the company is committed to expanding its services and presence in this region.

9 Technology Convergence Critical for PCB Fabrication

The PCB industry is showing signs of life, which indicates that the pendulum is swinging in a more positive direction economically, but we're not quite ready to uncork the champagne. A June 2013 report by Research & Markets forecast that the global PCB fabrication industry alone will reach about $94 billion in 2017, with a compounded annual growth rate (CAGR) of 8.1% during this period.

10 Multilayer Technology Nets 2014 Best of Irving Award

Various sources of information were gathered and analyzed to choose the winners in each category. The 2014 Irving Award Program focuses on quality, not quantity. Winners are determined based on the information gathered both internally by the Irving Award Program and data provided by third parties.

EVENTS

For the IPC Calendar of Events, click here.

For the SMTA Calendar of Events, click here.

For the iNEMI Calendar of Events, click here.

For the complete PCB007 Calendar of Events, click here.

SEMICON West TechXPOT: Driving Automotive Innovation
July 8–10, 2014
San Francisco, California, USA

Ohio Expo & Tech Forum
July 17, 2014
Cleveland, Ohio, USA

SusTech 2014
July 24–26, 2014
Portland, Oregon, USA

Advancements in Thermal Management 2014
August 6–7, 2014
Denver, Colorado, USA

Philadelphia Expo & Tech Forum
August 12, 2014
Cherry Hill, New Jersey, USA

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Printed Electronics

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New Concepts and Emerging Technologies for PCB Fabrication

October:
TBA